Features

- Max. ±19,999 counts

- QFP-44L and DIP-40L package

- Input full scale range: 200mV or 2V

- Built-in multiplexed **LCD** display driver

- Underrange/Overrange outputs

- 10μV resolution on 200mV scale

- Display Hold

- Precise 10:1 range select

- True differential input and reference

- Single power supply

- Built-in inverters for RC oscillation circuit

Application

Digital Multi-Meter

Description

ES5129 is a 19,999-count analog-to-digital converter (ADC) with multiplexed **LCD** display driver. It drives 4-1/2 digits, 4 decimal points, polarity, continuity and low battery indicator segments. ES5129 requires a typical 9V power supply for ADC operation. And it generates a COMMON reference for analog circuit and a DGND reference for digital circuit and LCD driver circuit. ES5129 has a ±19,999 counts resolution on both 200.00mV and 2.0000V ranges. It features high impedance inputs, excellent differential linearity, true ratiometric operation and auto polarity. The only external active component required is a reference. The underrange and overrange outputs and the 10:1 range changing inputs facilitate the design of autoranging systems. Other features include low battery detection, continuity check, Display Hold and controllable decimal points.

Pin Assignment

DIP-40L

OSC1 —	1	40 — OSC2
OSC3 —	2	39 — DP1
ANNUNC —	3	38 — DP2
B1, C1, CONT —	4	37 — RANGE
A1, G1, D1 —	5	36 — DGND
F1, E1, DP1 —	6	35 — REF_LO
B2, C2, LBAT —	7	34 — REF_HI
A2, G2, D2 —	8	33 — IN_HI
F2, E2, DP2 —	9	32 — IN_LO
B3, C3, MINUS —	10	31 — BUFFER
A3, G3, D3 —	11	30 — CREF-
F3, E3, DP3 —	12	29 — CREF+
B4, C4, BC5 —	13	28 — COMMON
A4, G4, D4 —	14	27 — CONTINUITY
F4, E4, DP4 —	15	26 — CINT
BP3 —	16	25 — CAZ
BP2 —	17	24 — V+
BP1 —	18	23 — V-
VDISP —	19	22 — HOLD
DP4/OR —	20	21 — DP3/UR

ES5129E

Pin Description

DIP-40L

Pin No	Symbol	Type	Description
1	OSC1	I	Input to first clock inverter.
2	OSC3	O	Output of second clock inverter.
3	ANNUNC	O	Backplane squarewave output for driving annunctors.
4	B1, C1, CONT	O	Output to LCD segment.
5	A1, G1, D1	O	Output to LCD segment.
6	F1, E1, DP1	O	Output to LCD segment.
7	B2, C2, LBAT	O	Output to LCD segment.
8	A2, G2 ,D2	O	Output to LCD segment.

9	F2, E2, DP2	O	Output to LCD segment.
10	B3, C3, MINUS	O	Output to LCD segment.
11	A3, G3, D3	O	Output to LCD segment.
12	F3, E3, DP3	O	Output to LCD segment.
13	B4, C4, BC5	O	Output to LCD segment.
14	A4, G4, D4	O	Output to LCD segment.
15	F4, E4, DP4	O	Output to LCD segment.
16	BP3	O	LCD backplane signal
17	BP2	O	LCD backplane signal
18	BP1	O	LCD backplane signal
19	VDISP	P	Negative supply for display drivers.
20	DP4/OR	I/O	Input: Turns on most significant decimal point when HI. Output: Pulled HI when result count exceeds ±19,999.
21	DP3/UR	I/O	Input: Turn on the 2nd significant decimal point when HI. Output: Pulled HI when result count is less than ±1,000.
22	LATCH/HOLD	I/O	Input: when floating, ES5129 operates in the free-run mode. When pulled high, the last display reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. Output: Negative going edge occurs when the data latche are upgraded. Can be used as a converter status signal.
23	V-	P	Negative power supply terminal
24	V+	P	Positive power supply terminal
25	CAZ	I/O	Integrator amplifier input
26	CINT	I/O	Integrator amplifier output
27	CONTINUITY	I/O	Input: when LO, continuity flag on the display is off. When HI, continuity flag is on. Output: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	COMMON	O	Set common-mode voltage of 3.2V below V+.
29	CREF+	I/O	Positive connection to external reference capacitor
30	CREF-	I/O	Negative connection to external reference capacitor
31	BUFFER	O	Buffer amplifier output
32	IN_LO	I	Negative input voltage terminal
33	IN_HI	I	Positive input voltage terminal
34	REF_HI	I	Positive reference voltage terminal
35	REF_LO	I	Negative reference voltage terminal
36	DGND	O	Ground reference for digital section
37	RANGE	I	Pulled HIGH externally for 2V scale.
38	DP2	I	When HI, decimal point 2 will be on.
39	DP1	I	When HI, decimal point 1 will be on.
40	OSC2	I/O	Output of first clock inverter. Input of second clock inverter.

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Pin Assignment

QFP-44L
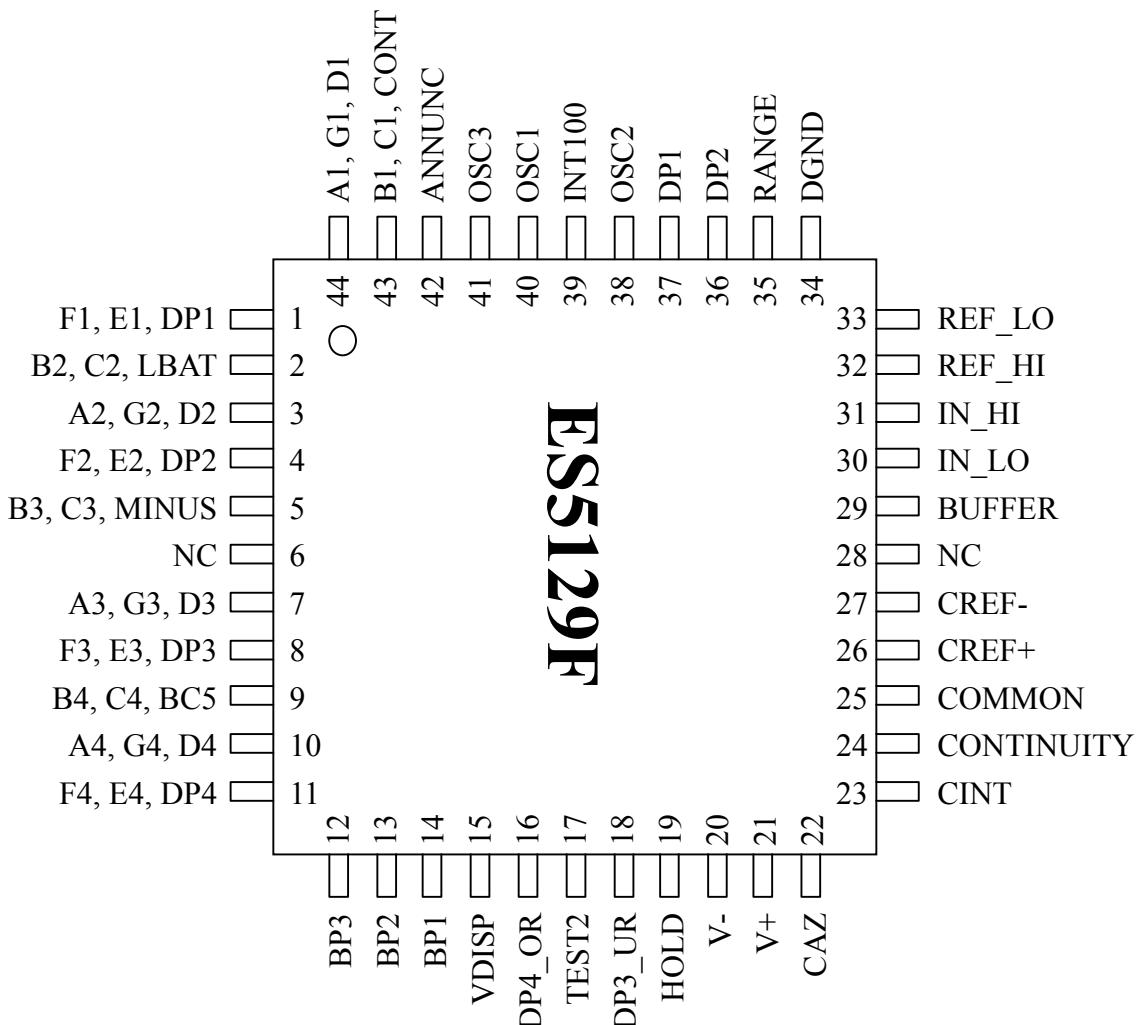
Pin Description

QFP-44L

Pin No	Symbol	Type	Description
1	F1, E1, DP1	O	Output to LCD segment.
2	B2, C2, LBAT	O	Output to LCD segment.
3	A2, G2 ,D2	O	Output to LCD segment.
4	F2, E2, DP2	O	Output to LCD segment.
5	B3, C3, MINUS	O	Output to LCD segment.
6	NC		
7	A3, G3, D3	O	Output to LCD segment.
8	F3, E3, DP3	O	Output to LCD segment.
9	B4, C4, BC5	O	Output to LCD segment.

10	A4, G4, D4	O	Output to LCD segment.
11	F4, E4, DP4	O	Output to LCD segment.
12	BP3	O	LCD backplane signal
13	BP2	O	LCD backplane signal
14	BP1	O	LCD backplane signal
15	VDISP	P	Negative supply for display drivers.
16	DP4/OR	I/O	Input: Turns on most significant decimal point when HI. Output: Pulled HI when result count exceeds ±19,999.
17	TEST2	O	TEST pin. Not connect.
18	DP3/UR	I/O	Input: Turn on the 2nd significant decimal point when HI. Output: Pulled HI when result count is less than ±1,000.
19	LATCH/HOLD	I/O	Input: when floating, ES5129 operates in the free-run mode. When pulled high, the last display reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. Output: Negative going edge occurs when the data latches are upgraded. Can be used as a converter status signal.
20	V-	P	Negative power supply terminal
21	V+	P	Positive power supply terminal
22	CAZ	I/O	Integrator amplifier input
23	CINT	I/O	Integrator amplifier output
24	CONTINUITY	I/O	Input: when LO, continuity flag on the display is off. When HI, continuity flag is on. Output: HI when voltage between inputs is less than +200mV LO when voltage between inputs is more than +200mV.
25	COMMON	O	Set common-mode voltage of 3.2V below V+.
26	CREF+	I/O	Positive connection to external reference capacitor
27	CREF-	I/O	Negative connection to external reference capacitor
28	NC		
29	BUFFER	O	Buffer amplifier output
30	IN_LO	I	Negative input voltage terminal
31	IN_HI	I	Positive input voltage terminal
32	REF_HI	I	Positive reference voltage terminal
33	REF_LO	I	Negative reference voltage terminal
34	DGND	O	Ground reference for digital section
35	RANGE	I	Pulled HIGH externally for 2V scale.
36	DP2	I	When HI, decimal point 2 will be on.
37	DP1	I	When HI, decimal point 1 will be on.
38	OSC2	I/O	Output of first clock inverter. Input of second clock inverter.
39	INT100	I	Reduce the integration time to 1/10 when RANGE is set to high. The polarity of ADC will be ignored also.
40	OSC1	I/O	Input of first clock inverter.
41	OSC3	I/O	Output of second clock inverter.
42	ANNUNC	O	Backplane squarewave output for driving annunctors.
43	B1, C1, CONT	O	Output to LCD segment.
44	A1, G1, D1	O	Output to LCD segment.

Absolute Maximum Ratings

Characteristic	Rating
Supply Voltage (V+ to V-)	15V
Analog Input Voltage	V- -0.6 to V+ +0.6
V+	V+ $\geq$ (AGND/DGND+0.5V)
AGND/DGND	AGND/DGND $\geq$ (V- -0.5V)
Digital Input	V- -0.6 to DGND +0.6
Power Dissipation. Flat Package	500mW
Operating Temperature	0℃ to 70℃
Storage Temperature	-25℃ to 125℃

Electrical Characteristics

TA=25℃, 9V between V+ and V-

Parameter	Test Condition	Min.	Typ.	Max	Units
Zero input reading	Vin=0, 200mV scale	-1	0	1	counts
Ratiometric reading	Vin=Vref=1V Range=2V	9998	9999	10000	counts
Rollover Error	+Vin=-Vin=199mV	—	—	2	counts
Linearity Error	200mV Scale	—	—	1	counts
Common Voltage	V+ to Common	2.8	3.2	3.5	V
Common Sink Current	$\triangle$common=+0.1V Sink current form V+	0.1	2		mA
Common Source Current	$\triangle$common=-0.1V Source current to V-	10	200		μA
DGND Voltage	V+ to DGND, V+ to V- =9V	4.5	5	5.5	V
DGND Sink Current	$\triangle$DGND=+0.5V Sink current form V+	0.6	-		mA
Supply Current excluding LCD display current	V+ to V- = 9V	—	1.0	1.4	mA
Supply Voltage Range	V+ to V-	6.7	9	14	V
Low Battery Flag	V+ to V-	6.9	7.2	7.5	V

07/03/01

Function Description

1. Normal Operation

When ES5129 operates at the oscillation frequency of 120KHz, the conversion period will be 500ms. And the less frequency it has, the longer time it takes to complete one conversion. ES5129 takes input signal from pins IN_LO and IN_HI differentially, and takes reference from pins REF_LO and REF_HI. The typical reference voltage is about 1V. A filter capacitor and a protective resistor are recommended at IN_HI and IN_LO terminal as the test circuit of page7.

2. Range Change Function

ES5129 has 2 operation ranges such as 200.00mV and 2.0000V. When the pin RANGE is pulled to DGND or keep floating, ES5129 operates at 200.00mV full-scale range. When it is pulled to V+, ES5129 change the input full-scale range to 2.0000V. And the output data still remain the maximum counting number ±20,000.

3. Data Hold Function

ES5129 support a data hold function to stop the LCD panel upgrading and hold the final data. When the pin HOLD keeps floating, ES5129 operates in free run mode, and the data upgrades automatically after every conversion. When it is pulled to V+, ES5129 enters HOLD mode, the LCD panel stops upgrading the output data, And the final data before the HOLD mode is activated is held.

4. Decimal Points Controlled

ES5129 can drive 4 decimal points on LCD panel. It provides four pins DP1, DP2, DP3 and DP4 to control the decimal points. Connect these pins DP1~DP4 to V+ will turn on the relative decimal point. To turn it off, keep DP pin float or connect it to DGND.

5. Continuity

An internal comparator with a 200mV threshold is connected directly between IN_LO and IN_HI pins. The continuity output will be pulled high whenever the voltage between the analog inputs is less than 200mV. And the "Continuity" annunciator on LCD panel will be turned on. To disable the continuity function, connect the pin continuity to DGND.

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6. Low Battery Detection

The Low Battery annunciator on the LCD panel turns on when the voltage drop between V+ and V- is below 7.2V.

7. LCD Display Configuration
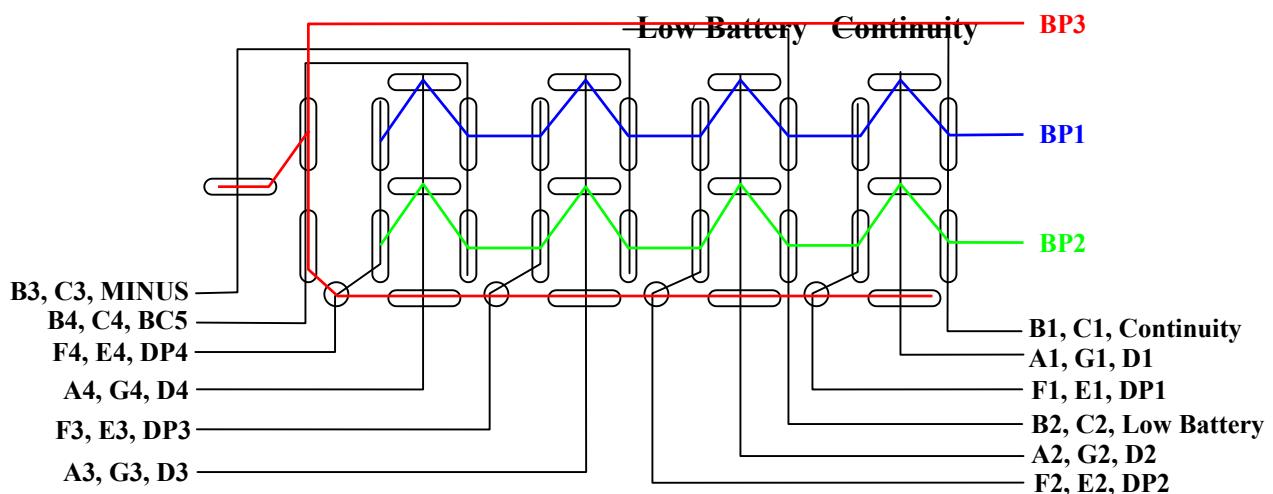
BP1	B1	A1	F1	B2	A2	F2	B3	A3	F3	B4	A4	F4
BP2	C1	G1	E1	C2	G2	E2	C3	G3	E3	C4	G4	E4
BP3	CONT	D1	DP1	LBAT	D2	DP2	MINUS	D3	DP3	BC5	D4	DP4
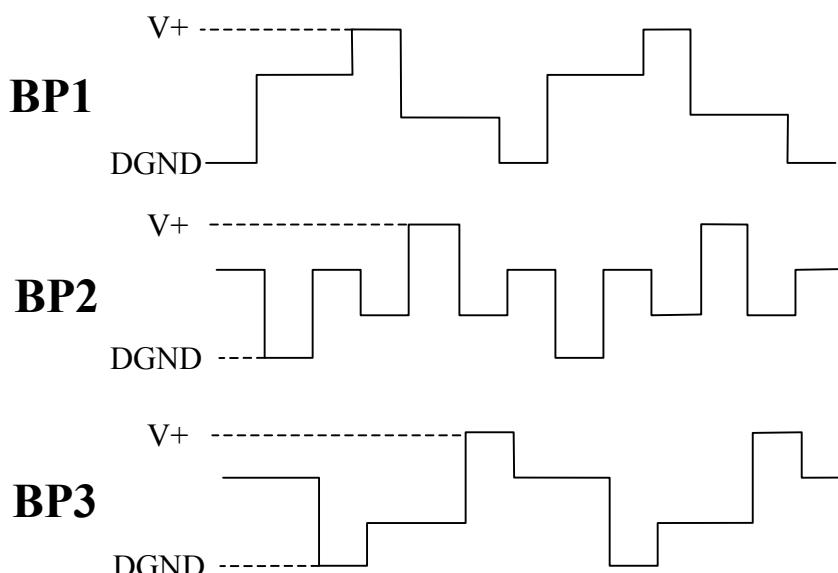
Test Circuit - with 120KHz crystal oscillator
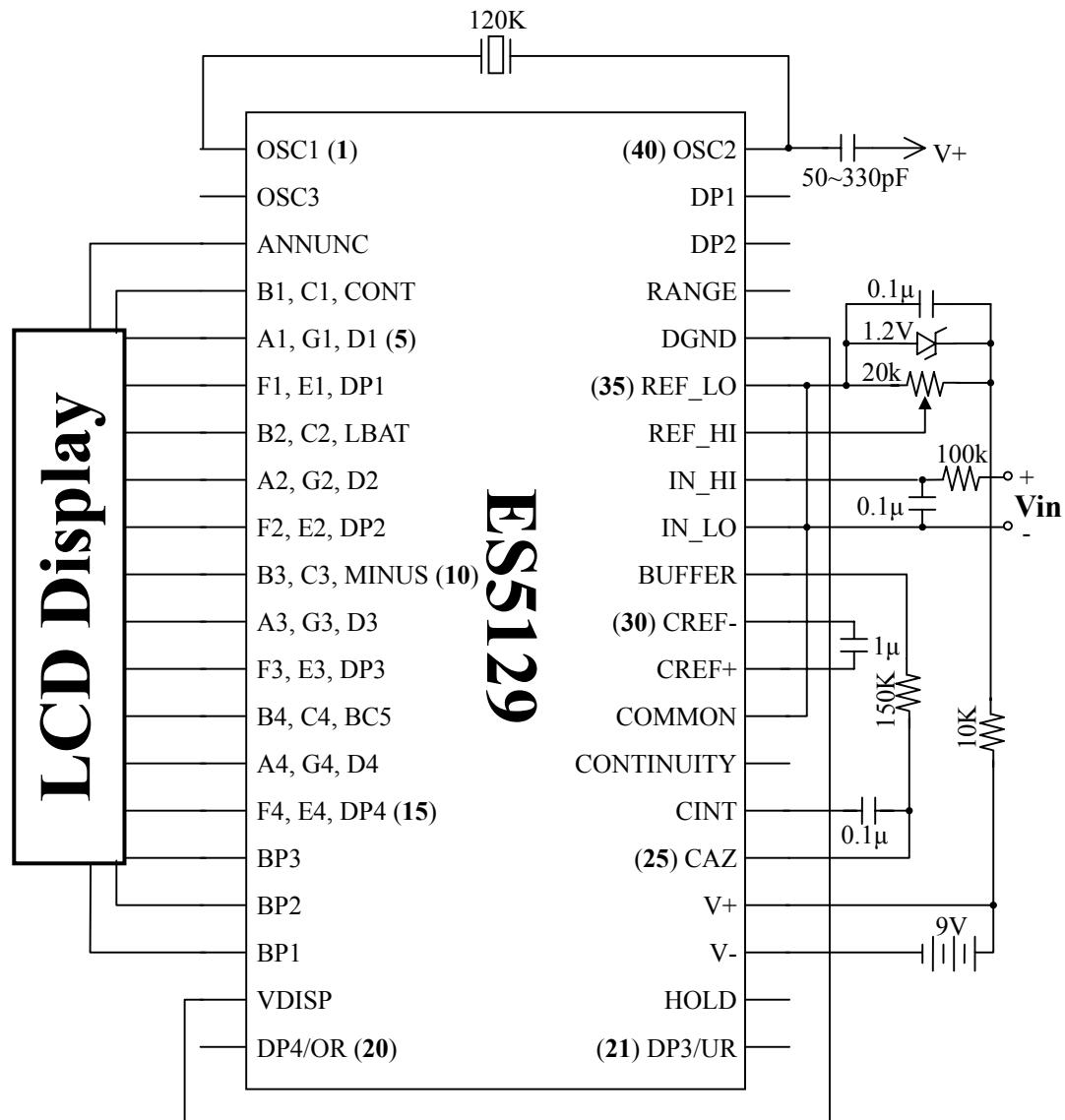
Test Circuit - with RC oscillation circuit

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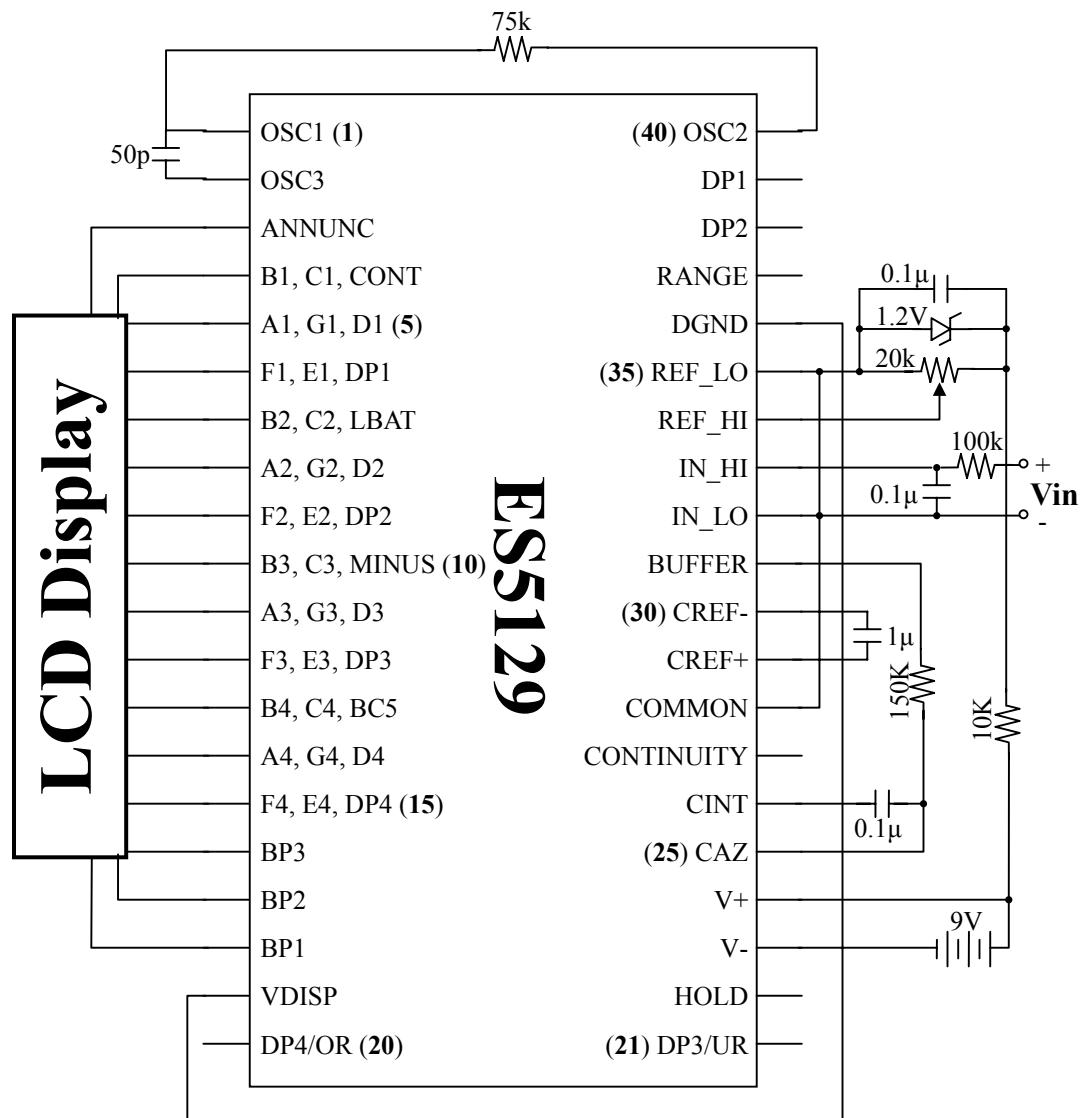
Product Outline: DIP-40L
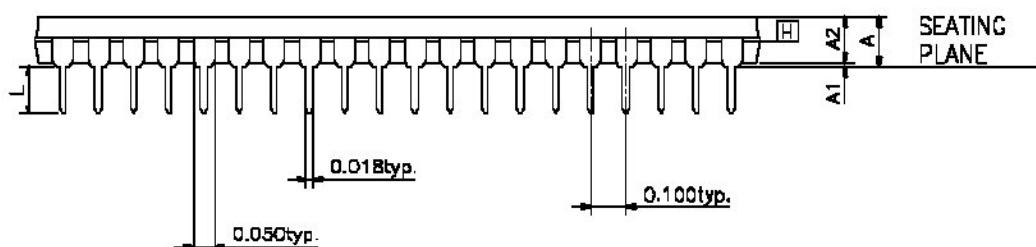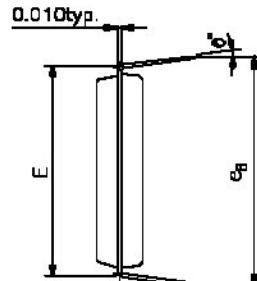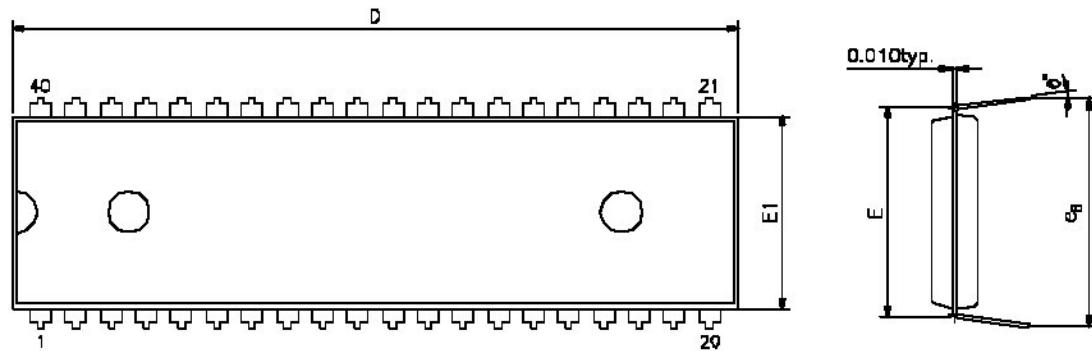
SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.190
A1	0.015	–	–
A2	0.150	0.155	0.160
D	2.055	2.060	2.070
E		0.600 BSC	
E1	0.540	0.545	0.550
L	0.120	0.130	0.140
e_B	0.630	0.650	0.670
θ	0	7	15

UNIT : INCH

NOTE:
1.JEDEC OUTLINE : MS-011 AC

Product Outline: QFP-44
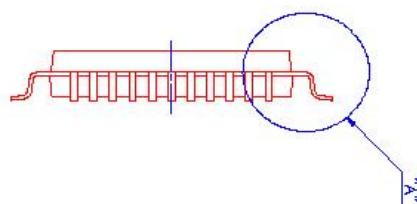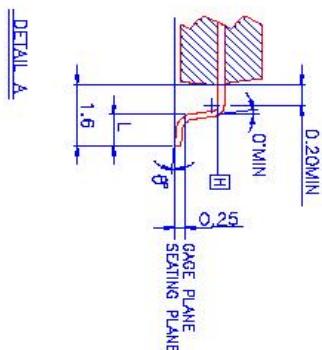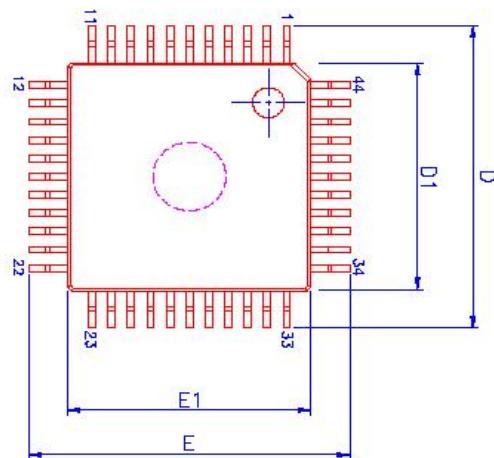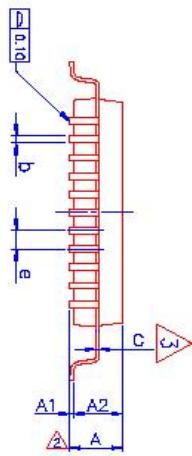
SYMBOLS	MIN.	NOM	MAX.
A	–	–	2.7
A1	0.25	0.30	0.35
A2	1.9	2.0	2.2
b	0.3 (TYP.)		
D	13.00	13.20	13.40
D1	9.9	10.00	10.10
E	13.00	13.20	13.40
E1	9.9	10.00	10.10
L	0.73	0.88	0.93
e	0.80 (TYP.)		
θ°	0	–	7
C	0.1	0.15	0.2

UNIT : mm

NOTES:

1. JEDEC OUTLINE:MO-108 AA-1

2. DATUM PLANE Ⓗ IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE Ⓗ.

4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.