承永資訊科技
CYRUSTEK CO.

ES51993
11,000 Counts ADC

Features

- Max. 11,000 counts resolution
- Conversion rate selectable by MPU command: 1.6/s → 128/s
- Input signal full scale: 110mV
- 50/60Hz line noise rejection selectable by MPU command
- Low battery detection
- Multiple input channels for ADC
- 3-wire serial bus and EOC signal for MPU I/O port
- -3V power operation with internal charge pumping circuit
- MPU I/O power level selectable by external control pin
- Support Peak Hold with calibration mode (**Taiwan patent no.: 476418**)
- Zero calibration for eliminating offset error
- On-chip buzzer driving and frequency selectable by MPU command
- Support sleep mode by external CS(chip-select) pin

Application

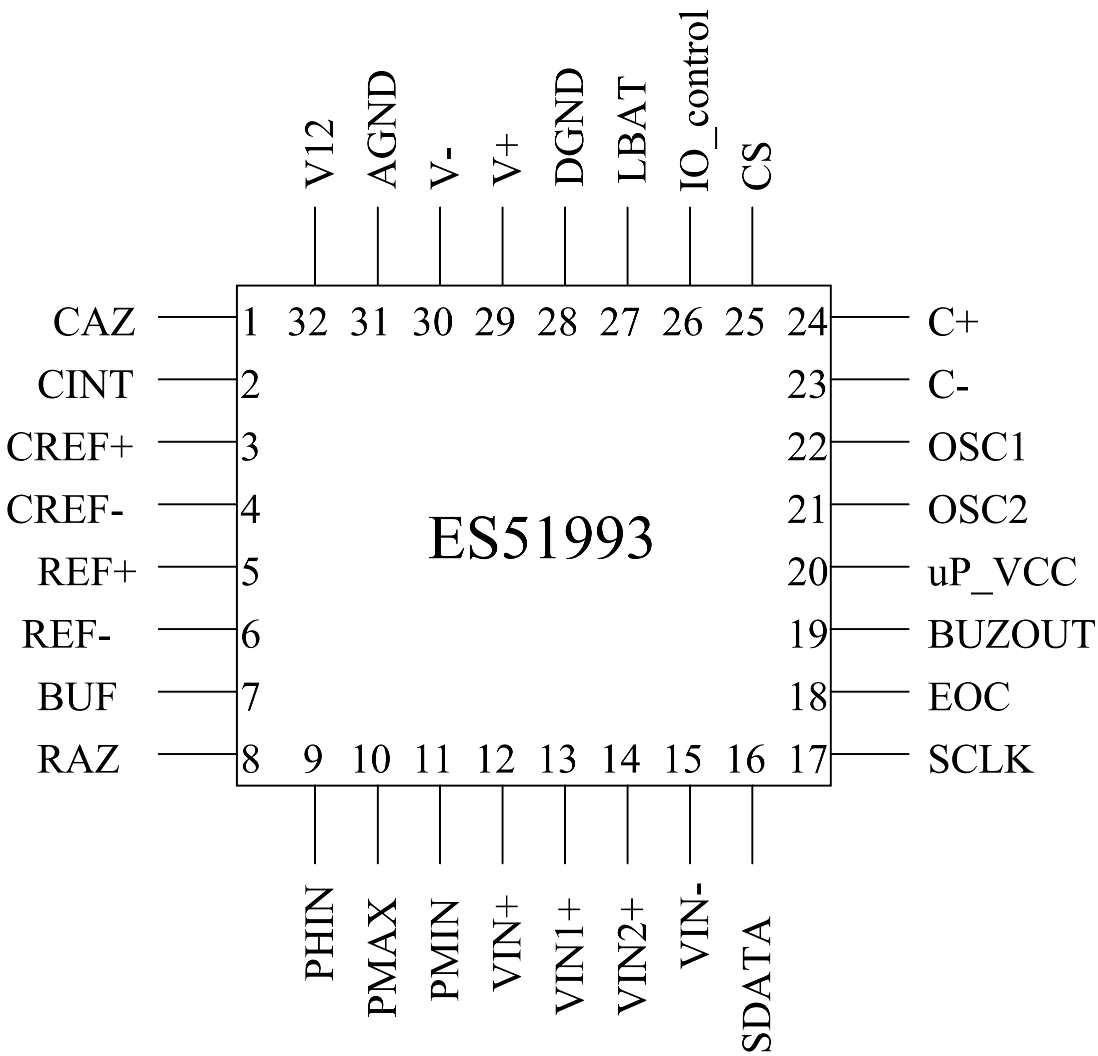
Clamp meter
Thermometer
Portable instrumentation

Description

ES51993 is an 11000-count dual-slope analog-to-digital converter (ADC) with peak hold function. The conversion rate and buzzer frequency can be selected or decided by an external microprocessor. The conversion rate can be varied from 1.6 time/sec to 128 times/sec under 4MHz/12MHz crystal oscillation clock. Besides, ES51993 also provides multi-channel input, low battery detection, power-down mode, 50/60Hz line noise rejection selection, and I/O port level selection for flexible design.

Pin Assignment

LQFP-32L



Pin Description

Pin No	Symbol	Type	Description
1	CAZ	I	Auto-zero capacitor connection.
2	CINT	O	Integrator output. Connect to integral capacitor
3	CREF+	I/O	Positive connection for reference capacitor.
4	CREF-	I/O	Negative connection for reference capacitor.
5	REF+	I	Differential reference high voltage input.
6	REF-	I	Differential reference low voltage input.
7	BUF	O	Buffer output pin. Connect to integral resistor
8	RAZ	O	Buffer output pin in high-speed mode. Connect to high-speed integral resistor.
9	PHin	I	Pick hold signal input which is reference to AGND
10	PMAX	O	Minimum peak hold output capacitor connection.
11	PMIN	O	Maximum peak hold output capacitor connection.
12	VIN+	I	Analog differential high signal input.
13	VIN1+	I	Analog signal high input1
14	VIN2+	I	Analog signal high input2
15	VIN-	I	Analog differential low signal input.
16	SDATA	I/O	Serial data I/O pin. Nch open-drain output.
17	SCLK	I	Serial clock input pin.
18	EOC	O	An indicator for ADC conversion ending.
19	BUZOUT	O	Buzzer frequency output
20	uP_VCC	I	MPU I/O port power level selection
21	OSC2	O	Crystal oscillation connection
22	OSC1	I	Crystal oscillation connection
23	C-	O	Negative capacitor connection for on-chip DC-DC converter.
24	C+	O	Positive capacitor connection for on-chip DC-DC converter.
25	CS	I	Chip select input pin. Pull to Low to enter power down mode.
26	I/O_control	I	MPU I/O port ground level selection
27	LBAT	I	Low battery configuration. If 3V battery is used, connect it to AGND. The default low-battery threshold voltage is –2.3V. If 9V or other battery voltage is used, the low battery annunciator is displayed when the voltage of this pin is less than V12
28	DGND	G	Digital ground
29	V+	O/P	Output of on-chip DC-DC converter.
30	V-	P	Negative supply voltage. Connecting to 3V battery negative terminal.
31	AGND	G	Analog ground
32	V12	O	Output of band-gap voltage reference. Typically –1.23V

Function description

1. Dual Slope A/D－Four Phases Timing

ES51993 is a dual-slope analog-to-digital converter (ADC). Figure 1 is a structure of dual-slope integrator. Its measurement cycle has two distinct phases: input signal integration (INT) phase and reference voltage integration (DINT) phase.

In INT phase, the input signal is integrated for a fixed time period, then A/D enters DINT phase in which an opposite polarity constant reference voltage is integrated until the integrator output voltage becomes to zero. Since both the time period for input signal integration and the amount of reference voltage are fixed, thus the de-integration time is proportional to the input signal. Hence, we can define the mathematical equation about input signal, reference voltage integration (see Figure 1.):

$$\frac{1}{Buf \times C\,\mathrm{int}} \int_0^{T_{INT}} V_{IN}(t)dt = \frac{1}{Buf \times C\,\mathrm{int}} \times V_{REF} \times T_{DINT}$$

where, $V_{IN}(t)$ = input signal
V_{REF} = reference voltage
T_{INT} = integration time (fixed)
T_{DINT} = de-integration time (proportional to $V_{IN}(t)$)

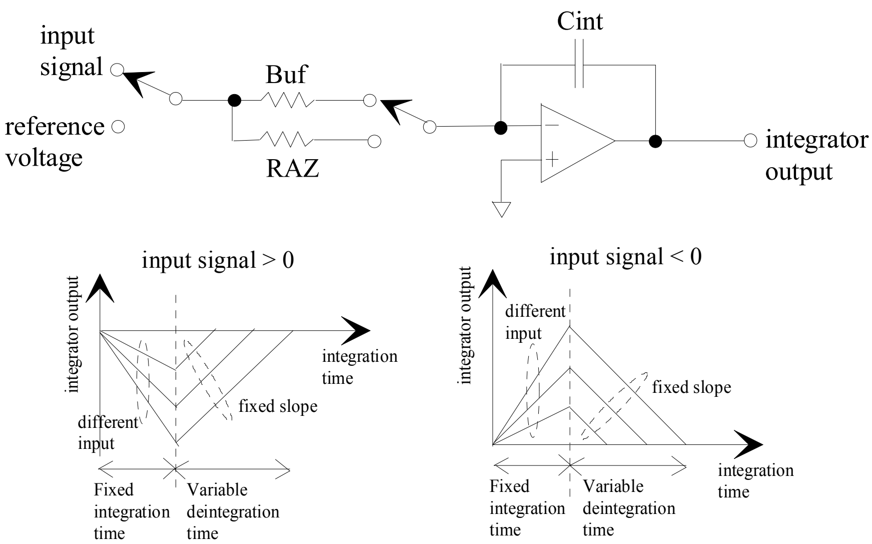


Figure 1. the structure of dual-slope integrator and its output waveform.

If $V_{IN}(t)$ is a constant, we can rewrite above equation:

$$T_{DINT} = \frac{T_{INT}}{V_{REF}} \times V_{IN}$$

Besides the INT phase and DINT phase, ES51993 exploits auto zero (AZ) phase and zero integration (ZI) phase to achieve accurate measurement. In AZ phase, the system offset is stored. The offset error will be eliminated in DINT phase. Thus a higher accuracy could be obtained. In ZI phase, the internal status will be recovered quickly to that of zero input. Thus the succeeding measurements won't be disturbed by current measurement especially in case of overload.

As mentioned above, the measurement cycle of ES51993 contains four phases:

(1) auto zero phase (AZ)
(2) input signal integration phase (INT)
(3) reference voltage integration phase (DINT)
(4) zero integration phase (ZI)

The time ratios of these four phases, AZ, INT, DINT and ZI to the entire measurement cycle are 8.8%, 32%, 35.2% and 24% respectively. However the actual duration of each phase depends on conversion rate. An example is shown in the table below. A user can easily deduce other cases based on the table.

Voltage:

CR (times/sec)	ZI (ms)	AZ (ms)	INT (ms)	DINT (ms)
8	**30**	**11**	**40**	**44**

Note: reference voltage = -100 mV.

Voltge+PEAK:

CR (times/sec)	ZI (ms)	AZ (ms)	INT (ms)	DINT (ms)
8	**30**	**11**	**40**	**60**

Note: reference voltage = -100 mV.

2. Component Value Selection for ADC

For various application requirements on conversion rate and input full range, we suggest nominal values for external components of ADC in Figure 1 to obtain better performance. Under default condition with operating clock = 12 MHz:

(1) conversion rate = 8 times/sec
(2) reference voltage = -100 mV
(3) input signal full scale = 110 mV (sensitivity = 10 uV)

We suggest that Cint = 68 nF, Buf = 56 kΩ

If a user selects a different conversion rate rather than default, the integration capacitor Cint value must be changed according to the following rule for better performance:

Cint × (conversion rate) = (68 nF) × (8 times/sec).

A smaller Cint reduces the input full range. However a larger Cint might have weaker noise immunity than the suggested one.

A user could enlarge the input full range by changing reference voltage (Vref) and the amount of integration resistor (Buf). For example, if Vref & Buf are enlarged as twice than the default values then the input full range becomes 220 mV. The input full range can be enlarged up to 1.1V (10 times than the default case). We list general rules in below which might be helpful in determining component values.

Buf / (reference voltage) = 56 kΩ / (-100 mV)

3. Multi Channel Input

ES51993 provides VIN+, VIN1+, VIN2+ and Vin- pins to achieve the multi channel input (multiplexer) feature. Because ES51993 is a single core A-to-D converter, it can only process one pack of data per conversion period. Although it has four input pins, it would take only one pair as input channel from the four pins. The actual input channel is determined by the bits CH1/CH0 of STATUS Byte1 as the following table:

Input Channel	CH1	CH0	High Input	Low Input
ch1	0	0	VIN+	VIN-
ch2	0	1	VIN1+	VIN-
ch3	1	0	VIN2+	VIN-
ch4	1	1	VIN2+	VIN1+

ES51993 also configures an input channel rotation (polling) feature. Setting the ROT bit of STATUS Byte2 to high can activate the rotation feature. In the rotation mode, the actual input channel will be changed by ES51993 sequentially and automatically. The rotation feature has two types, one is for three input channel rotation with the same low input, another one is for two independent differential channel rotation. The following table presents the configuration of the rotation type.

Rotation Type Table:

<table>
<tr><th>ROT</th><th>CH1,CH0</th><th>Rotation Type</th></tr>
<tr><td rowspan="4">H</td><td>0,0</td><td rowspan="3">ch1 → ch2 → ch3 → ch1 ⋯</td></tr>
<tr><td>0,1</td></tr>
<tr><td>1,0</td></tr>
<tr><td>1,1</td><td>ch1 → ch4 → ch1 ⋯</td></tr>
<tr><td>L</td><td>-</td><td>Not Rotating</td></tr>
</table>

4. Special function

4.1 Peak Hold

ES51993 provide a Peak Hold function to capture the REAL peak value for voltage or current measurement mode. In a case of a 1V sine wave input voltage, the Peak Hold function gets a PMAX value of 1.414V and PMIN value of –1.414V. Set the bit PEAK of STATUS byte3 to high to force the ES51993 enter PEAK mode.. In the PEAK mode, ES51993 takes high input from PHin and low input from AGND. Peak Hold function is divided into two parts of peak maximum and peak minimum conversion. ES51993 performs peak maximum and peak minimum conversion by turns, not at the same time. The bit PMAX and PMIN of STATUS Byte2 present which type the peak value is.

4.2 Peak Calibration

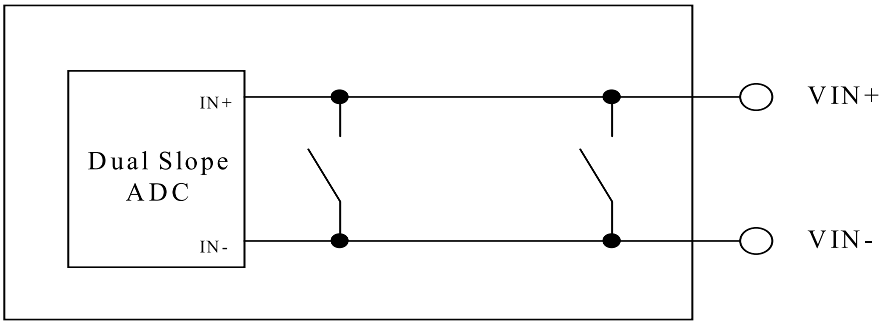
In PEAK mode, the offset voltage of internal OP Amps will cause an error. To obtain a more accurate value, this offset effect must be canceled. ES51993 provides the Peak Calibration feature to remove the influence on accuracy by internal offset voltage. Set the bit PCAL of STATUS Byte2 to high to enter Peak Calibration mode. In this mode, ES51993 will output the calibration value of peak maximum and minimum conversion by turns. The calibration value is the error rise from offset voltage, and it muse be recorded. In PEAK mode, the peak value must minus the calibration value to remove the error.

Note:

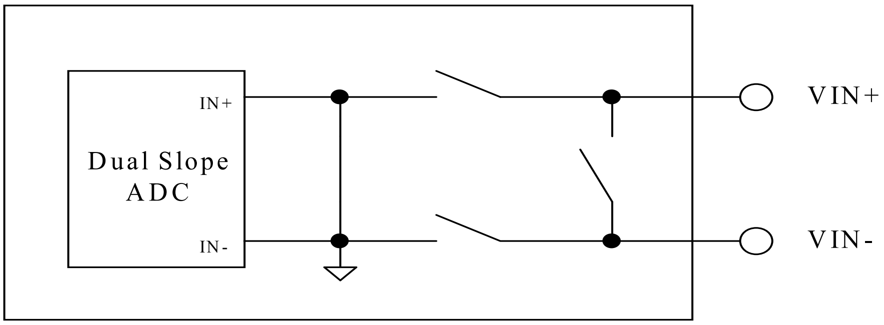
1. After entering Peak or PCAL mode, it is recommended to leave the Peak or PCAL mode first. Then wait one conversion time delay before change mode to PCAL or Peak mode, respectively. The time delay is necessary for normalizing the charge of P_{MAX}/P_{MIN} capacitor.
2. When buzzer control bit is active, the Peak & PCAL mode are not allowed.

4.3 Zero and RZero Calibration

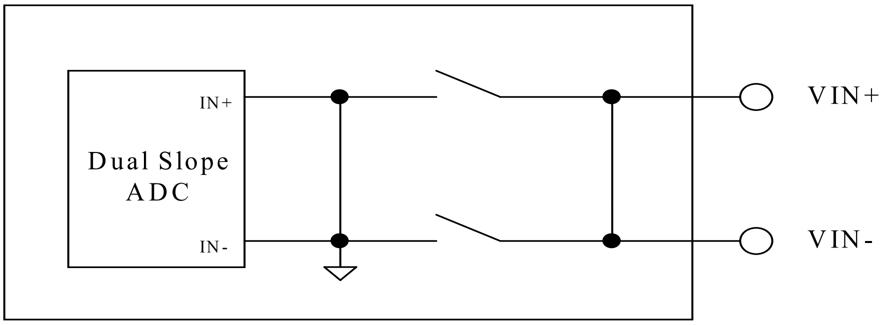
The Zero and RZero calibration are designed for removing the error rise from the propagation delay of internal component. In Zero or RZero calibration mode, ES51993 outputs a calibration value. The normal measurement value must minus the calibration value to cancel the error and obtain a more accurate value. The following block diagram performs the difference between basic structures of normal mode, Zero calibration and RZero Calibration. We suggest users to do zero-calibration in most applications.



(a) Normal mode



(b) Zero mode



(c) RZero mode

4.4 Buzzer Setup

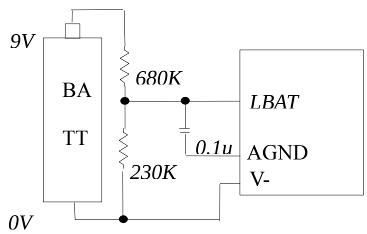
When the bit **BUZ** of ID Byte is set to “H”, the BUZOUT will output a square signal of MPU I/O swing level to drive a external buzzer. The buzzer frequency is determined by the bits B0/B1/B2 of STATUS Byte3. The configuration of buzzer frequency is listed at the following table.

B2/B1/B0	BUZout (kHz)
111	4.00
110	3.33
101	3.08
100	2.67
011	2.22
010	2.00
001	1.33
000	1.00

4.5 Low Battery Detection

In a case of 3V battery power, the pin LBAT must be shorted to AGND. And the system will have low battery detection level about 2.3V. In another case of 9V or other battery power, the low battery detection happens when the voltage of LBAT is less than –1.23V below GND. And the bit LBAT of STATUS Byte3 will be set to high. A recommended application is shown as following:

Low battery test (9V)



The low battery detection level is around 7V

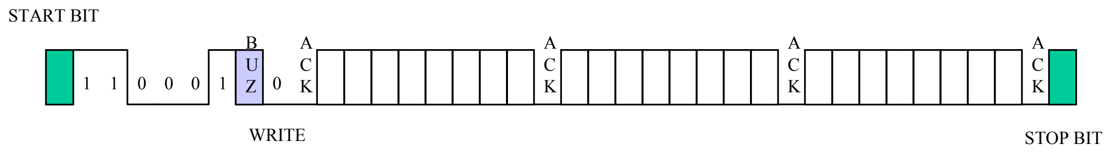
4.6 Sleep Mode

When the pin CS is connected to V- or GND (depended on I/O_control level), the ES51993 will enter sleep mode. In Sleep mode, the chip draws a little supply current. It could extend the battery life. To leave sleep mode or stay in normal mode, the pin CS must be connected to AGND or floating.

5. MPU I/O functional definition

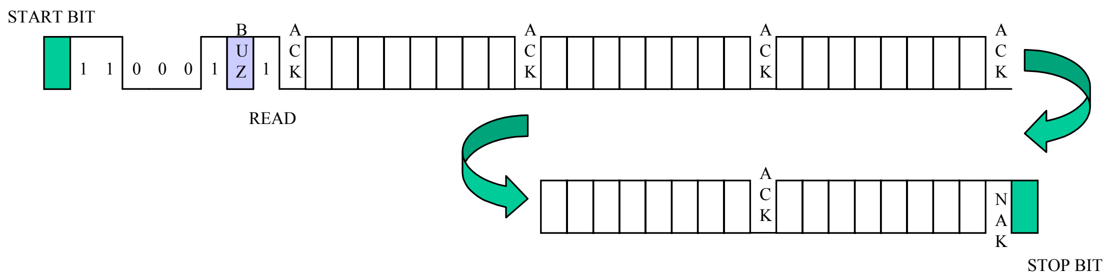
Write command:

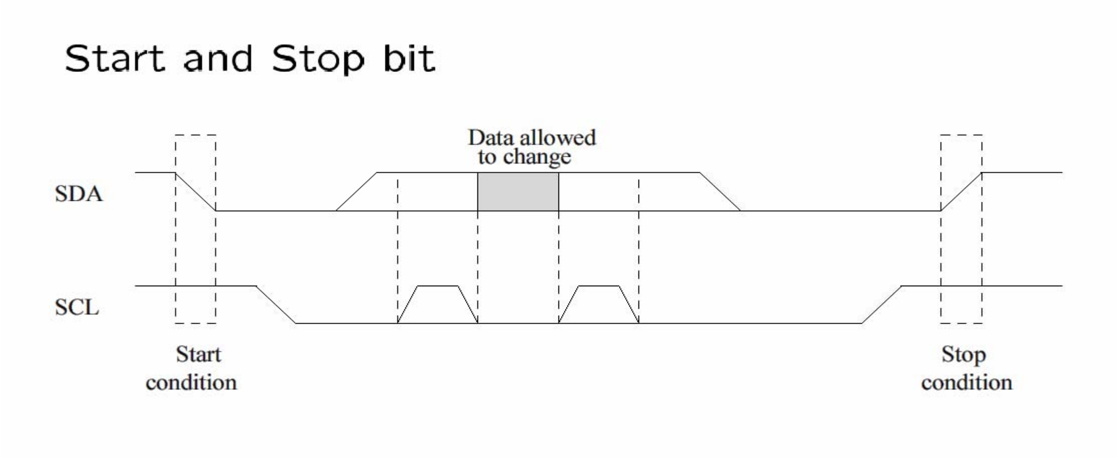
ID byte, Status byte1, Status byte2, Status byte3



Read command:

ID byte, Status byte1, Status byte2, Status byte3, Data byte1, Data byte2





ID byte:

1	**1**	**0**	**0**	**0**	**1**	**BUZ**	**R/W**

Status byte1:

CH0	**CH1**	**C0**	**C1**	**C2**	**SIGN**	**SEL4M**	**X**

Status byte2:

S60	**RZERO**	**ZERO**	**ROT**	**PMAX**	**PMIN**	**X**	**X**

Status byte3:

PEAK	**PCAL**	**B0**	**B1**	**B2**	**LBAT**	**X**	**X**

Data byte1:

D0	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**

Data byte2:

D8	**D9**	**D10**	**D11**	**D12**	**D13**	**X**	**X**

R/W: set to "H" is in read mode, set to "L" is in write mode

CH1/CH0: ADC input channel selection, the default is [00].

Code	VIN(+)	VIN(-)
00	VIN0 channel	VIN- channel
01	VIN1 channel	VIN- channel
10	VIN2 channel	VIN- channel
11	VIN2 channel	VIN1 channel

C2/C1/C0/S60: Conversion rate selection, the default is [0000]

C2/C1/C0	S60	
	L	H
101	128/s	128/s
100	96/s	96/s
011	64/s	76.8/s
010	32/s	38.4/s
001	16/s!	19.2/s*
000	8/s!	9.6/s*
110	3.2/s!*	3.84/s*
111	1.6/s!*	1.92/s*

Crystal: 12MHz

!: 50Hz line noise rejection, *: 60Hz line noise rejection

SEL4M: "H" is XTAL is 4MHz version, "L" is default 12MHz XTAL

C2/C1/C0	S60
	X
101	128/s
100	64/s
011	64/s
010	32/s
001	16/s!
000	8/s!
110	3.2/s!*
111	1.6/s!*

Crystal :4MHz

SIGN: "H" is negative, "L" is positive

PMAX: "H" is maximum peak value, the default is "L"

PMIN: "H" is minimum peak value, the default is "L"

LBAT: "H" is low battery detection flag active, the default is "L"

PEAK: "H" is peak hold function turn on, the default is "L"

PCAL: "H" is peak hold function calibration mode is active, the default is "L"

RZERO: "H" is RZero calibration mode "ON", the default is "L"

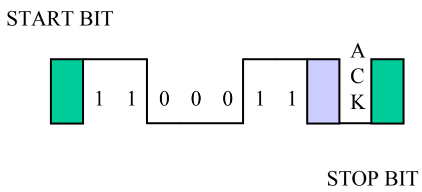
ZERO: “H” is Zero calibration mode “ON”, the default is “L”

ROT: Set to ”H” to enable multi channel rotating feature

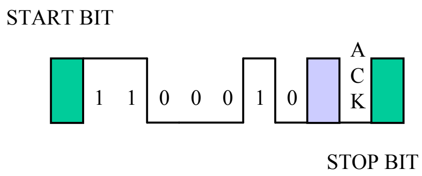
B2/B1/B0: Buzzer frequency selection (independent with conversion rate)

BUZ: “H” is buzzer turn on and “L” is turn off, the default is turn off.

Buzzer ON



Buzzer OFF



D13-D0: ADC output data according channel multiplex [CH1/CH0]. Binary code format.

6. Power and I/O output level selection

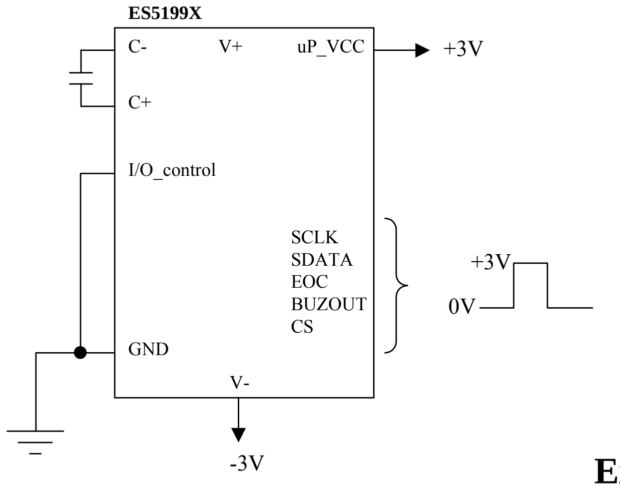
Power

- Charge pump output for positive supply voltage(V+)
- External DC source to V+ is available by floating the charge pump capacitor

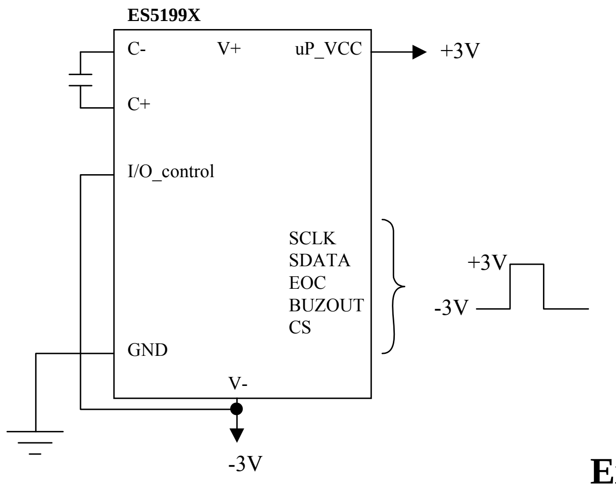
I/O output level selectable

- uP_VCC provided by external DC source (the same high level with MPU)
- A control pin (I/O_control) selects the low level to –3V(V-) or 0V(DGND)

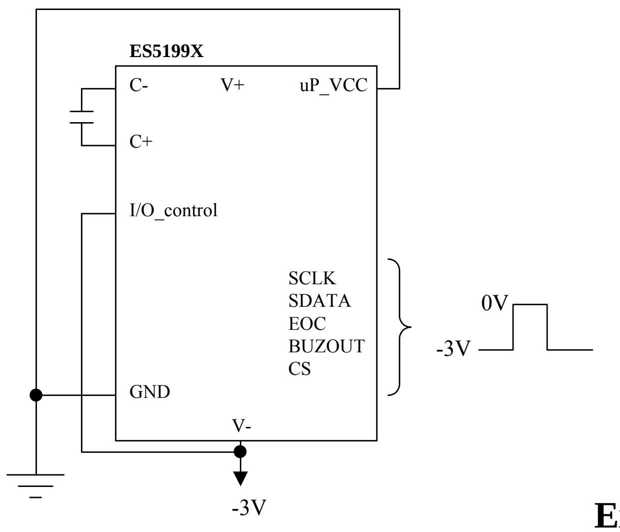
uP_VCC	I/O_control	I/O level		Example
		H	L	
3	H	+3V	0V	Ex.1
3	L	+3V	-3V	Ex.2
0	L	0V	-3V	Ex.3


ES5199X
C-
V+
uP_VCC
+3V
C+
I/O_control
SCLK
SDATA
EOC
BUZOUT
CS
+3V
0V
GND
V-
-3V

Ex.1


ES5199X
C-
V+
uP_VCC
+3V
C+
I/O_control
SCLK
SDATA
EOC
BUZOUT
CS
+3V
-3V
GND
V-
-3V

Ex.2


ES5199X
C-
V+
uP_VCC
C+
I/O_control
SCLK
SDATA
EOC
BUZOUT
CS
0V
-3V
GND
V-
-3V

Ex.3

Absolute Maximum Ratings

Characteristic	Rating
Supply Voltage (V- to AGND)	-3.6V
Analog Input Voltage	V- -0.6 to V+ +0.6
V+	V+ ≥ (AGND/DGND+0.5V)
AGND/DGND	AGND/DGND ≥ (V- -0.5V)
Digital Input	V- -0.6 to DGND +0.6 or V+ +0.6
Power Dissipation. Flat Package	500mW
Operating Temperature	0℃ to 70℃
Storage Temperature	-25℃ to 125℃

DC Electrical Characteristics

TA=25℃, V_{CM} = 0V, V-=-3V

Parameter	Symbol	Test Condition	Min.	Typ.	Max	Units
Power supply	V-		-3.3	-3.0	-2.5	V
Operating supply current Conversion rate = 8/sec.	I_{DD}	Normal operation (XTAL=12MHz)	—	2.0	2.2	mA
	I_{SS}	In sleep mode	—	2.5	5	µA
Voltage roll-over error	REV		—	—	±0.05	%F.S[1]
Voltage nonlinearity	NLV	Best case straight line	—	—	±0.05	%F.S
Input Leakage				1	10	pA
Low battery flag voltage		V- to AGND	-2.4	-2.3	-2.2	V
Internal pull-high to uP_Vcc current		CS (uP_Vcc=3V)		5		uA
		CS(uP_Vcc=0V)		1.5		
Internal pull-low to V- current		I/O_control (V-=-3V)		1.5		uA
Zero input reading		10MΩ input resistor zero cal. by MPU	-000	000	+000	counts
Reference voltage and open circuit voltage for 110Ω measurement	V_{REF}	100KΩ resistor between VRH and AGND	-1.33	-1.23	-1.13	V
Reference voltage temperature coefficient	TC_{RF}	100KΩ resister Between VRH 0℃<TA<70℃	—	50	—	ppm/℃
Minimum pulse width for Peak Hold feature	T_{PW}		100			µs

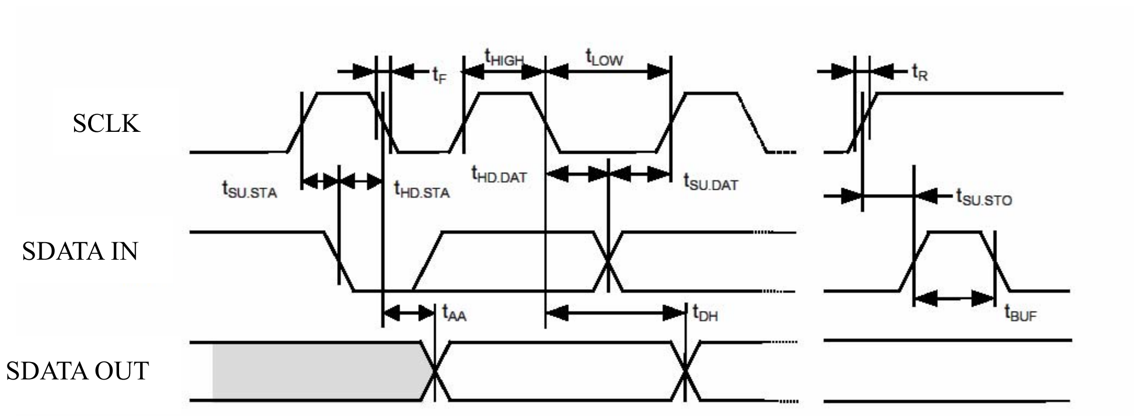
Note:

1.Full Scale

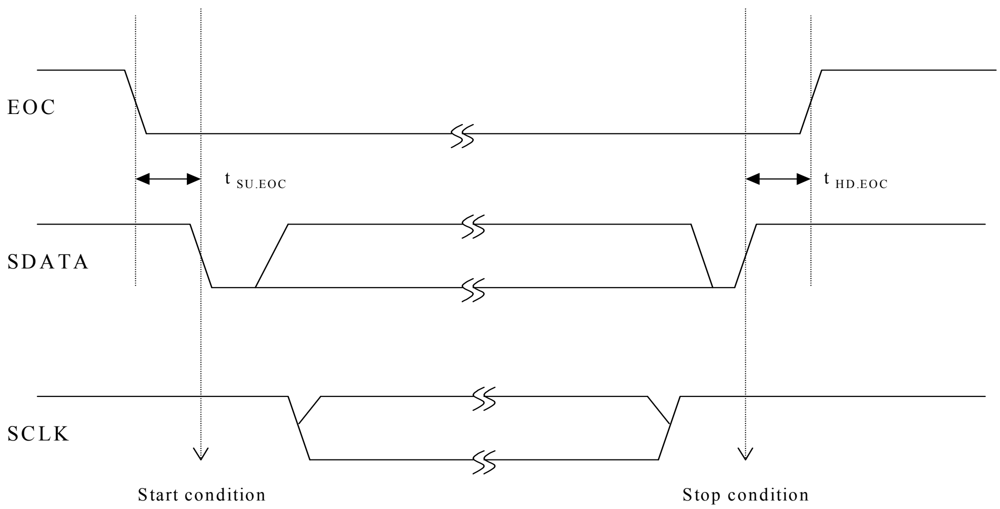
AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCLK clock frequency	f_{SCLK}	-	-	100	kHz
SCLK clock time "L"	t_{LOW}	4.7	-	-	
SLCK clock time "H"	t_{HIGH}	4.0	-	-	us
SDATA output delay time	t_{AA}	0.1	-	3.5	
SDATA output hold time	t_{DH}	100	-	-	ns
Start condition setup time	$t_{SU.STA}$	4.7	-	-	us
Start condition hold time	$t_{HD.STA}$	4.0	-	-	
Data input setup time	$t_{SU.DAT}$	200	-	-	ns
Data input hold time	$t_{HD.DAT}$	0	-	-	
Stop condition setup time	$t_{SU.STO}$	4.7	-	-	
SCLK/SDATA rising time	t_R	-	-	1.0	us
SCLK/SDATA falling time	t_F	-	-	0.3	
Bus release time	t_{BUF}	4.7	-	-	
EOC setup time in read mode	$t_{SU.EOC}$	0			ns
EOC hold time in read mode	$t_{HD.EOC}$	0	-	-	ns

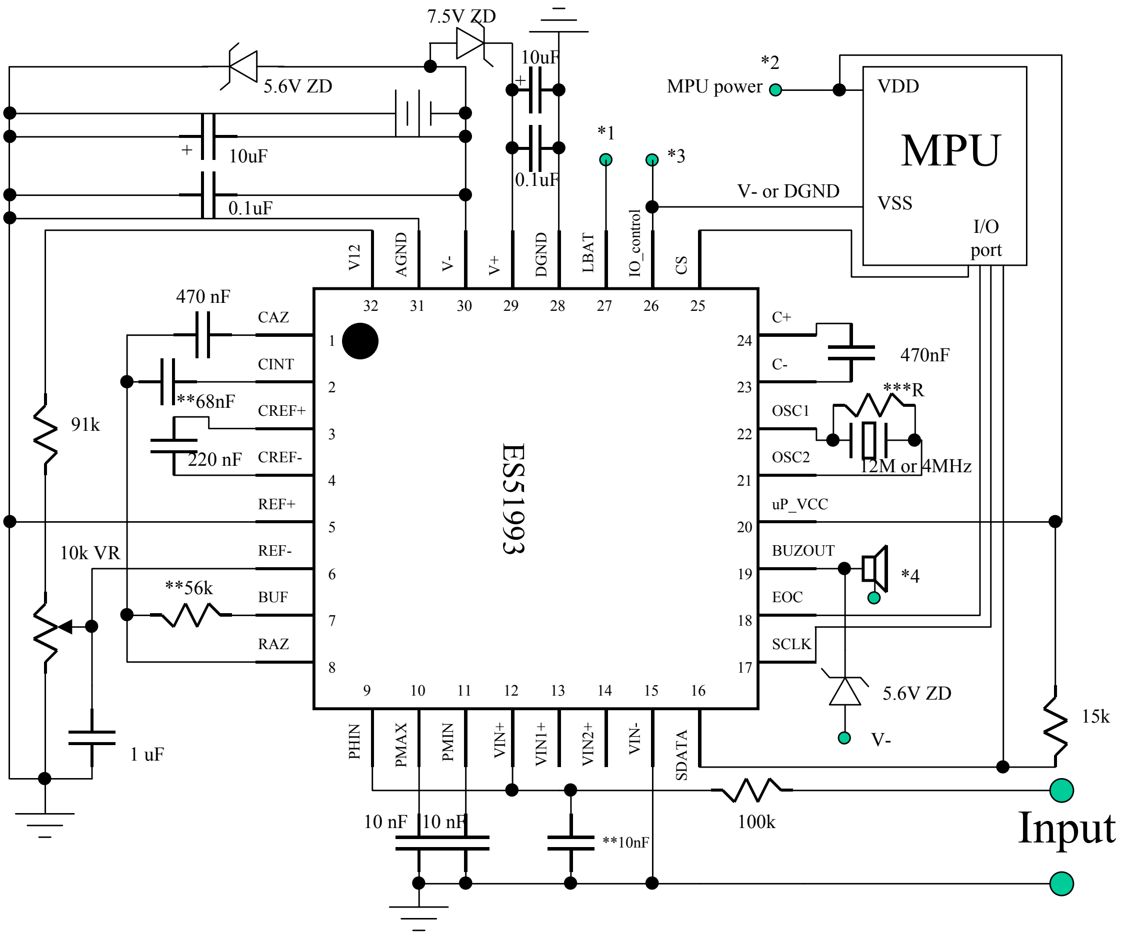
I/O timing diagram



Read mode EOC timing diagram



Application example



Note:

Zener diodes in above circuit are used for IC protection, so MUST be soldered on PCB first.

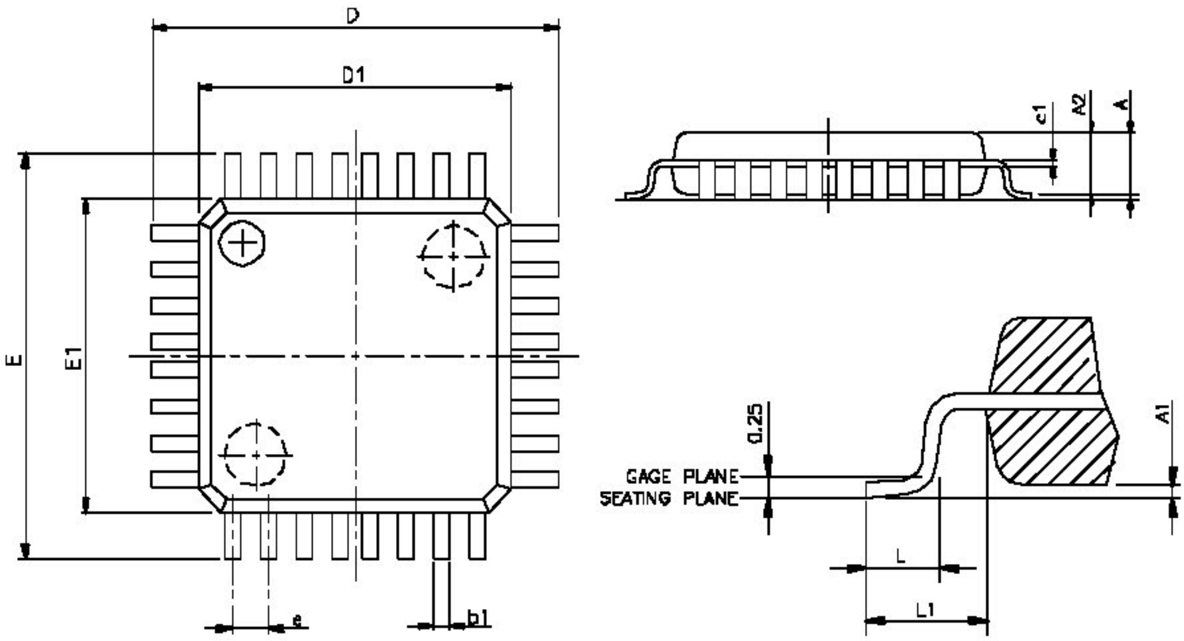
***1*2*3*4: Depend on power design**

**** Depends on conversion rates setting: V-= -3.0V**

(a)Conversion rate	(b)C_{INT}(uF)	(c)R_{BUF}(kΩ)	(a)Conversion rate	(b)C_{INT}(uF)	(c)R_{BUF}(kΩ)
128/s	0.01	22	16/s	0.068	27
96/s	0.01	30	9.6/s	0.047	68
76.8/s	0.01	39	8/s	0.068	56
64/s	0.022	22	3.84/s	0.1	82
38.4/s	0.022	36	3.2/s	0.1	91
32/s	0.033	27	1.92/s	0.22	68
19.2/s	0.033	47	1.6/s	0.22	91

***** R=10~22MΩ resistor is optional**

Product Outline: LQFP-32



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.8 BSC	
b	0.30	0.45
L	0.45	0.75
L1	1 REF	

NOTES:

1.JEDEC OUTLINE:MS-026 BBA

2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.