1 · GENERAL DESCRIPTION

The ES5120 is a 3 3/4 digit measurement system which combines integrating analog-to-digital converter, frequency counter,and logic level tester in either 40-pin DIP package or 44-pin QFP package · The high level of integration permits ES5120-based instruments to deliver higher performance and more features while actually reducing parts count.

With a maximum range of 3999 counts, the ES5120 provides 10 times greater resolution in the 200mV to 400mV range than traditional 3 1/2 digit meters. An autozero cycle guarantees a zero reading with a 0V input. CMOS Processing reduces analog input bias current to only 1PA. Rollover error, the difference in readings for equal magnitude but opposite polarity input signals, is less than ± 1 Count. Differential reference inputs permit ratiometric measurements for ohms or bridge transducer applications.

The ES5120's frequency counter option simplifies design of an instrument which is well suited to both analog and digital troubleshooting : voltage, current, and resistance measurements plus precise frequency measurements to 4 MHz (higher frequencies can be measured with an external prescaler) and a simple logic probe. The frequency counter will automatically adjust its range to match the input frequency, over a four decade range.

ES5120

3 3/4 DIGIT A/D CONVERTER

Two logic level measurement inputs permit a ES5120-based meter to function as a logic probe. When combined with external level shifters, the ES5120 will display logic levels on the LCD display and also turn on a piezoelectric buzzer when the measured logic level is low.

Other ES5120 features simplify instrument design and reduce parts count. On-chip decimal point drivers are included, as is a low battery detection annunciator. A piezoelectric buzzer can be controlled with an external switch or by the logic probe inputs.

Two oscillator options are provided : A crystal can be used if high accuracy frequency measurements are desired, or a simple RC option can be used for low-end instruments.

A 'peak reading hold' input allows the ES5120 to retain the highest A-D or frequency reading. This feature is useful in measuring motor starting current, maximum temperature, and similar applications.

The ES5120 operates from a single 9V battery, with typical power of 16mW. Packages include a 40-pin DIP and 44-pin Flat Package.

2 · FEATURES

- Multiple-Function Measurement System
  - Analog to digital Converter
  - Frequency Counter
  - Logic Probe
- Frequency Counter
  - Measures Input Frequency to 4 MHz
  - Autoranging Over Four Decade Range
- Logic Probe Inputs
  - 2 LCD Annunciators
  - Buzzer Drive (with Two Types of Buzzer Frequencies, 5 KHz and 2.5KHz, for choice)
- Peak Reading Hold with LCD Annunciator
- 3 3/4 Digit(3999 Maximum) Resolution
- Low Noise A-D Converter
  - Differential Inputs, 1 pA Bias Current
  - Differential Reference for Ratiometric Ohms
  - On-Chip Voltage Reference, 60 ppM/℃ Drift
- No External LCD Drivers Required
  - Full 3 3/4 Digit Display
  - Displays "OL" for Input Overrange

- Three Decimal Point and Polarity Drivers
- LCD Annunciator Drive
- Adjustable LCD Drive Voltage

■ Low Battery Detect with LCD Annunciator

■ On Chip Buzzer Driver and Control Input

■ Control Input Changes Full Scale Range by 10:1

■ Data Hold Input

■ Underrange and Overrange Outputs

■ Multiple Package Options

- 40-pin DIP Package
- 44-pin Flat Package

3 · TYPICAL APPLICATION

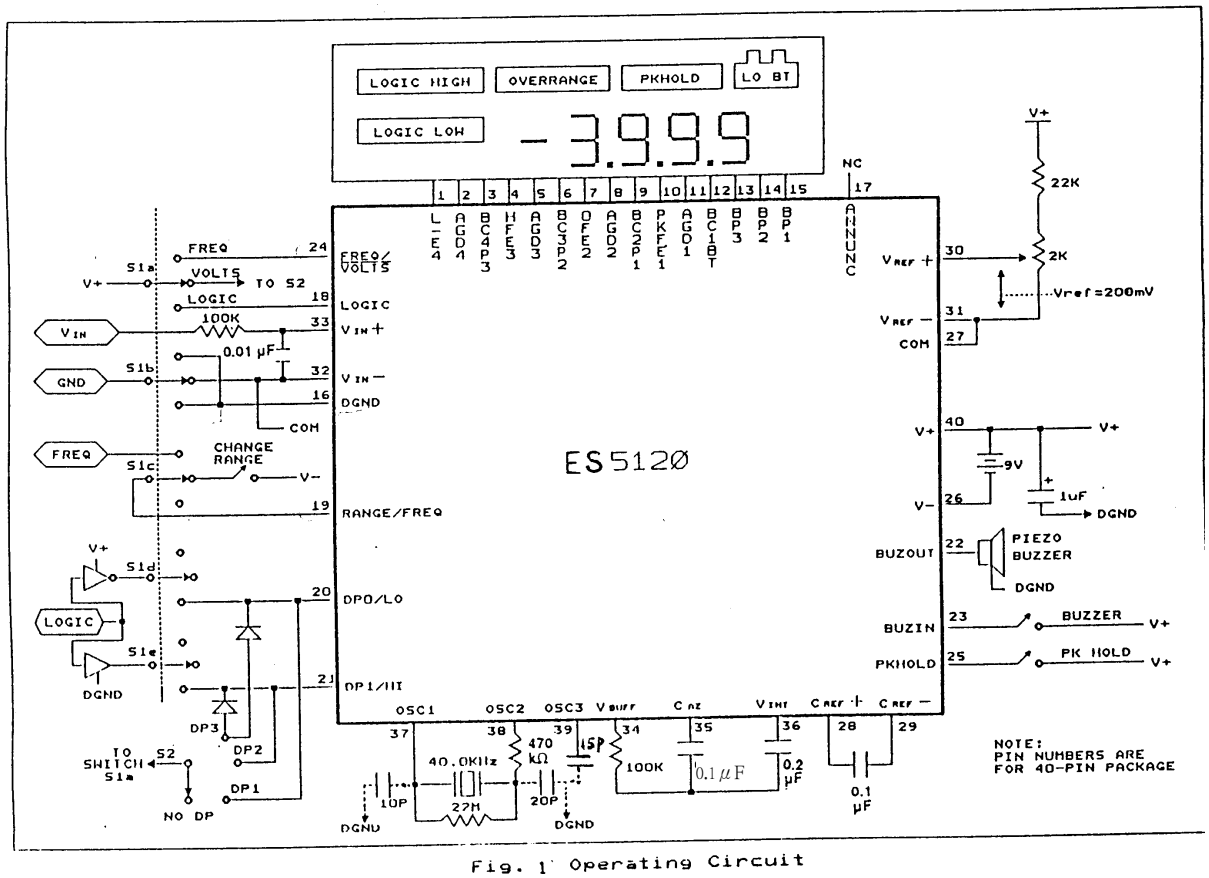


Fig. 1 Operating Circuit

4 · FUNCTIONAL BLOCK DIAGRAM

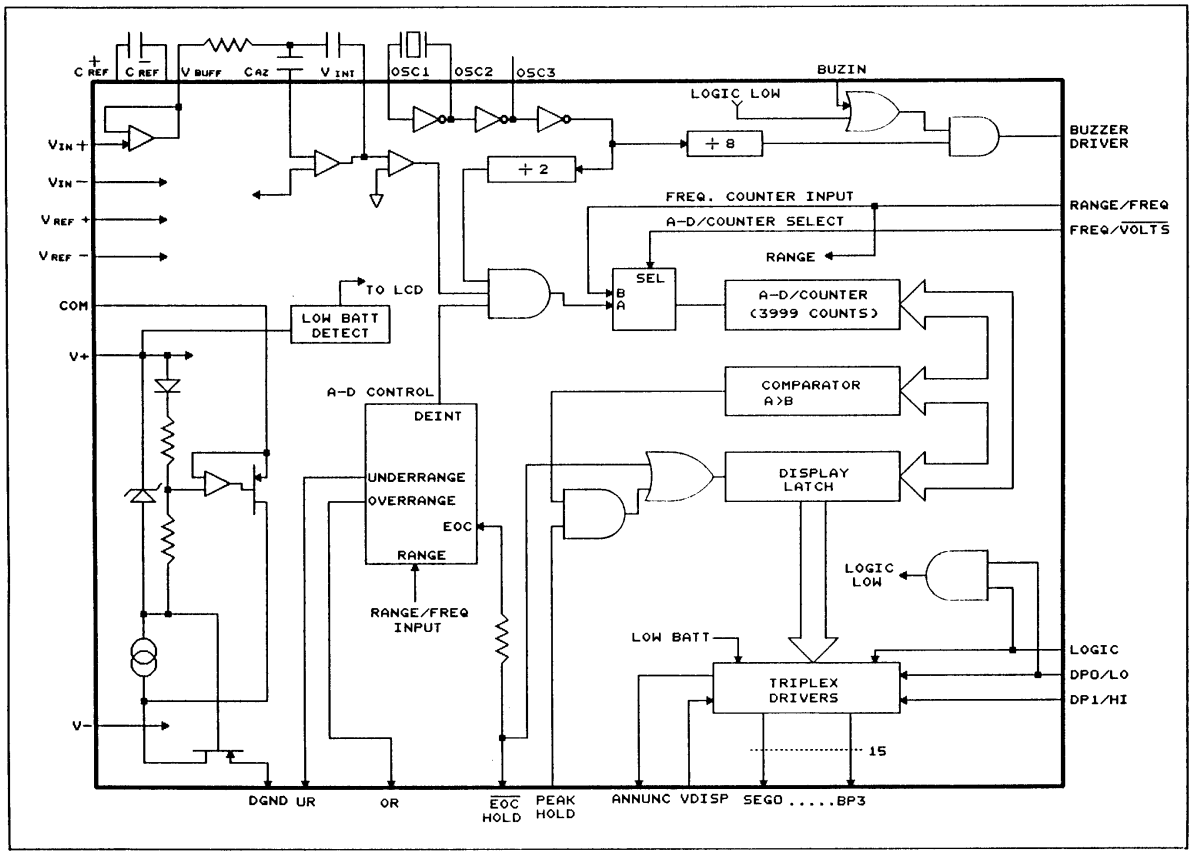
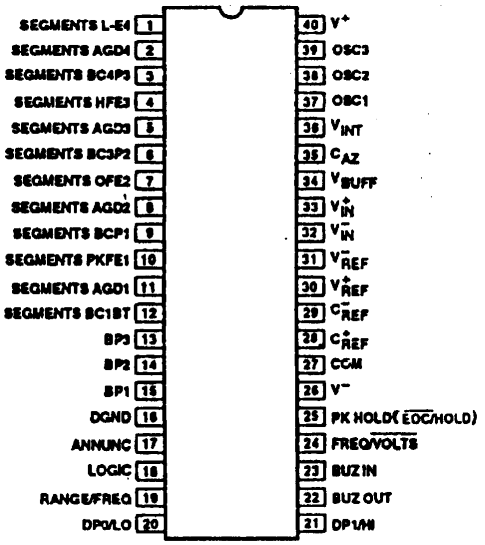


Fig. 2 Functional Block Diagram

5 · PIN ASSIGNMENT

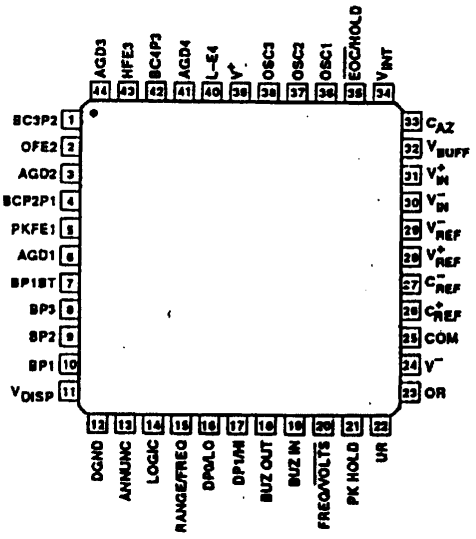


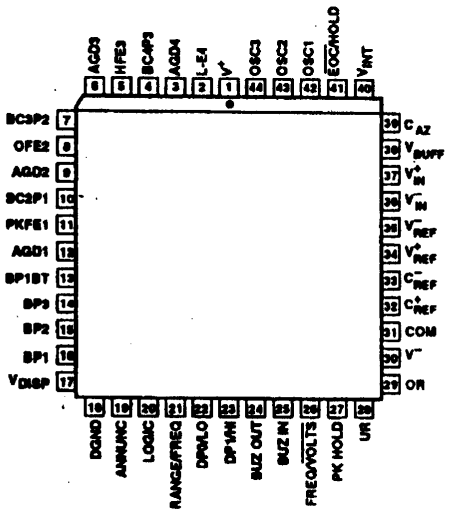
* 4 types of DIP Package :

	A	B	P	D
	Buzzer Freq. 2.5 KHz	Buzzer Freq. 5.0 KHz	Peak Hold (Pin 25)	Data Hold (Pin 25)
CIC5120ADE	V	-	-	V
CIC5120APE	V	-	V	-
CIC5120BDE	-	V	-	V
CIC5120BPE	-	V	V	-

* 2 types of Flat Package :

	A	B
	Buzzer Freq. 2.5 KHz	Buzzer Freq. 5.0 KHz
ES5120AQ	V	-
ES5120BQ	-	V





*2 types of PLCC Package :

	A	B
	Buzzer Freq. 2.5KHz	Buzzer Freq. 5.0KHz
ES5120AZ	V	-
ES5120BZ	-	V

6 · PIN DESCRIPTION AND FUNCTION

Pin No. (40-pin Package)	Pin No. (44-pin Flat Package)	Symbol	Descrlption
1	40	L-E4	LCD segment drive for L("logic low"),polarity,and"e"segment of most significant digit (MSD)
2	41	AGD4	LCD segment drive for"a","g",and"d"segments of MSD
3	42	BC4P3	LCD segment drive for"b"and"c"segments of MSD and decimal point 3
4	43	HFE3	LCD segment drive for H("logic high"), and"f"and"e"segment of 3rd LSD
5	44	AGD3	LCD segment drive for"a","g", and"d"segments of 3rd LSD
6	1	BC3P2	LCD segment drive for"b"and"c"segments of 3rd LSD and decimal point 2.
7	2	OFE2	LCD segment driver for"overrange",and"f"and"e"segments of 2nd LS
8	3	AGD2	LCD segment drive for"a","g",and"d"segments of 2nd LSD.
9	4	BC2P1	LCD segment drive for"b"and"c"segments of 2nd LSD and decimal point 1.
10	5	PKFE1	LCD segment drive for "hold peak reading", and"f"and"e"segments of LSD
11	6	AGD1	LCD segment drive for"a","g",and"d"segments of LSD.

Pin No. (40-pin Package)	Pin No. (44-pin Flat Package)	Symbol	Descrlption
12	7	BC1BT	LCD segment drive for"b"and"c"segments of LSD and "low battery".
13	8	BP3	LCD backplane #3.
14	9	BP2	LCD backplane #2.
15	10	BP1	LCD backplane #1.
	11	VDISP	Sets peak LCD drive signal : V_{PEAK}=(V+)-VDISP may also be set to compensate for temperature variation of LCD crystal threshold voltage.(default: The VDISP pin is connected to DGND.)
16	12	DGND	Internal logic digital ground, the logic "O" level. Nominally 4.7V below V＋
17	13	ANNUNC	Square wave output at the backplane frequency, synchronized to BP1 ANNUNC can be used to control display annunciators. Connecting an LCD segment to ANNUNC turns it on; connecting it to its backplane turns it off.
18	14	LOGIC	"Logic Mode" control input. When connected to V＋ the converter is in logic mode. The LCD displays "OL" and the decimal point inputs control the "high" and "low" annunciators. When the "low" annunciator is on, the buzzer will also be on. When unconnected or connected to DGND, the ES5120 is in the voltage frequency measurement mode. This pin has a 5 μA internal pulldown to DGND.

Pin No. (40-pin Package)	Pin No. (44-pin Flat Package)	Symbol	Descrlption
19	15	RANGE/ FREQ	Dual-purpose input.In voltage mode:When connected to V＋; the FREQ integration time will be 200 counts instead of 2000 counts,and the LCD will display the analog input divided by 10. In frequency mode, this pin is the frequency input. A digital signal applied to this pin will be measured with a one second timebase. There is an internal 5 μA pulldown to DGND.
20	16	DP0/LO	Dual-purpose input. Decimal Point select input for voltage measurements. In logic mode, connecting this pin to V＋ will turn on "low" LCD segment. There is an internal 5 μA pulldown to DGND in volts mode only. Decimal point logic: DP1 DP0 Decimal Point Selected 0 0 None 0 1 DP1 1 0 DP2 1 1 Dp3
21	17	DP1/HI	Dual-purpose input. Decimal Point select input for voltage measurements. In logic mode, connecting this pin to V＋ will turn on the "high" LCD segment. There is an internal 5 μA pulldown to DGND in volts mode only.
22	18	BUZOUT	Buzzer output. Audio frequency, 2.5K or 5.0K for choice determined by chip bonding, output which drives a piezo buzzer.

Pin No. (40-pin Package)	Pin No. (44-pin Flat Package)	Symbol	Descrlption
23	19	BUZIN	Buzzer control input. Connecting BUZIN to V＋ turns the buzzer on. BUZIN is logically ORed(internally) with the "logic level low" input. There is an internal 5 μA pulldown to DGND.
24	20	FREQ/ VOLTS	Voltage or frequency measurement select input. When connected to DGND, the a-d converter function is active. When connected to V＋ the frequency counter function is active. This pin has an internal 5 μA pulldown to DGND.
25	21	PKHOLD	Peak Hold input. When connected to V＋, the converter will only update the display if a new conversion value is greater than the preceeding value. Thus, the peak reading will be stored and held indefinitely. When unconnected or connected to DGND, the converter will operate normally. This pin has an internal 5 μA pulldown to DGND. (Note : This pin may be with the function of $\overline{\text{EOC}}$/HOLD which depends on chip bonding.)
	22	UR	Underrange output. This output will be high when the digital reading is 380 counts or less.
	23	OR	Overrange output. This output will be high when the analog signal input is greater than full scale. The LCD will display "OL" when the input is overranged.

Pin No. (40-pin Package)	Pin No. (44-pin Flat Package)	Symbol	Descrlption
26	24	V-	Negative supply connection. Connect to negative terminal of 9V battery.
27	25	COM	Analog circuit ground reference point. Nominally 3.3V below V＋.
28	26	C_{REF}^{+}	Positive connection for reference capacitor.
29	27	C_{REF}^{-}	Negative connection for reference capacitor.
30	28	V_{REF}^{+}	High differential reference input connection.
31	29	V_{REF}^{-}	Low differential reference input connection.
32	30	V_{IN}^{-}	Low analog input signal connection.
33	31	V_{IN}^{+}	High analog input signal connection.
34	32	V_{BUFF}	Buffer output. Connect to integration resistor.
35	33	C_{AZ}	Autozero capacitor connection.
36	34	V_{INT}	Integrator output. Connect to integration capacitor.
	35	$\overline{\text{EOC}}$/ HOLD	Bidirectional pin. Pulses low (i.e. from V+ to DGND) at the end of each conversion. If connected to V+, conversions will continue but the display is not updated.
37	36	OSC1	Crystal oscillator (input) connection.
38	37	OSC2	Crystal oscillator (output) connection.
39	38	OSC3	RC oscillator connection.
40	39	V+	Positive power supply connection. Typically 9V.

7 · ABSOLUTE MAXIMUM RATING

Characteristic	Rating
Supply Voltage (V^+ to V^-)	12 V
Analog Input Voltage (either input)	V^+ to V^- 1V
Reference Input Voltage (either input)	V^+ to V^- 1V
Digital Inputs	DGND to V^+
Power Dissipation (plastic package)	800 mW
Operating Temperature	0℃ to +70℃
Storage Temperature	-65℃ to +160℃
Lead Temperature (soldering, 10 sec)	270℃

※ Note：There are ten pins for Analog section, such as COM, C_{REF}^+,C_{REF}^-, V_{REF}^+, V_{REF}^-, V_{IN}^+, V_{IN}^-, V_{BUFF}, C_{AZ}, and V_{INT} and the others are related to Digital section.

8．ELECTRICAL CHARACTER ISTICS

At V+=9V，fosc 40KHZ，TA=25℃ unless otherwise noted

Characteristic	Test Conditions	Limit			Units
Zero Input Reading	V_{IN}＝0.0V Full-Scale=400.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN}=V_{REF}$ V_{REF}=200mV	1999	1999/ 2000	2000	Digital Reading
Linearity (Max. deviation from best straight line fit)	Full-Scale=400mV	-1	± 0.2	1	Counts
Roll-over Error	$-V_{IN}=+V_{IN}$=390.0mV	-1	± 0.2	+1	Counts
Common Mode Rejection Ratio	V_{CM}=± 1V, V_{IN}=0V Full-Scale=400.0mV	—	50	—	μV/V
Noise	V_{IN}=0V, Full-Scale=400.0mV	—	15	—	μVp-p
Zero Reading Drift	V_{IN}=0V 0℃≦T_A≦70℃	—	0.2	1	μV/℃
Scale Factor Temperature Coefficient	V_{IN}=399.0mV 0℃≦T_A≦70℃(Ext. Ref.= 0 ppm/℃	—	1	5	ppm/℃
Analog COMMON Voltage (with respect to V^+)	25KΩ between Common and Positive Supply	3.15	3.3	3.45	V
Analog COMMON Temperature Coefficient	25KΩ between Common and V^+ 0℃≦T_A≦70℃	—	30	50	ppm/℃
Back plane Drive Voltage(Peak To Peak)	V^+ to V^-＝9V	4.5	5.0	5.5	V
Supply Current (Does not include COMMON current)	V_{IN}＝0V	—	1.2	1.7	mA

ELECTRICAL CHARACTERISTICS (contd.)

Characteristic	Test Conditions	Limit			Units
		Min.	Typ.	Max.	
Buzzer Freguency	fosc = 40.0 KHz		5.0/2.5 *1		KHz
Counter Timebase Period	fosc = 40.0 KHz		1		second
Low Battery Flag Voltage	V^+ to V^-	6.7	7.0	7.3	V
Control pin Pulldown Current			5		μA

Note 1:Two types of Buzzer Frequencies for choice determined by chip bonding.

Characteristic	Test Conditions	Limit			Units
		Min.	Typ.	Max.	
Input Low Voltage		—	—	DGND +1.5V	V
Input High Voltage		V+ -1.5V	—	—	V
Output, Low Voltage UR、OR、Outputs	1_L=50uA	—	—	DGND +0.4V	V
Output High Voltage UR、OR Outputs	1_N=50uA	V+ -1.5V	—	—	V

9 · TEST CIRCUIT

9.1 General Function Test

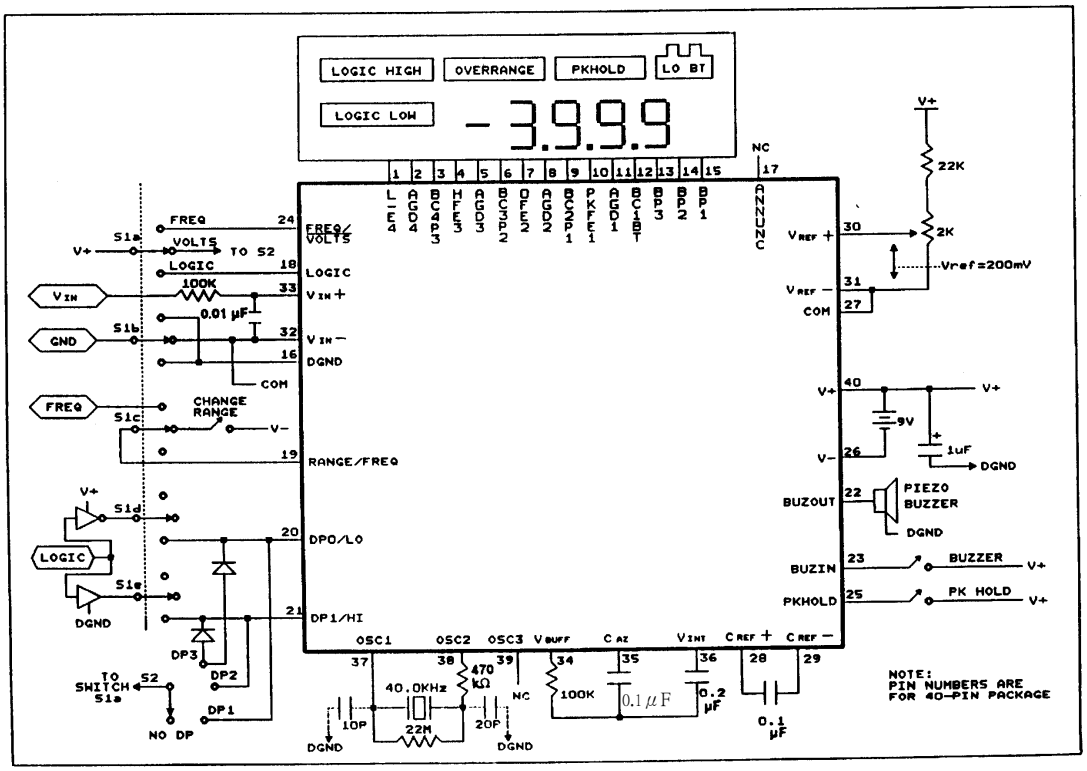


Fig.3 general Function Test Circuit

9.2 ICCQ Test

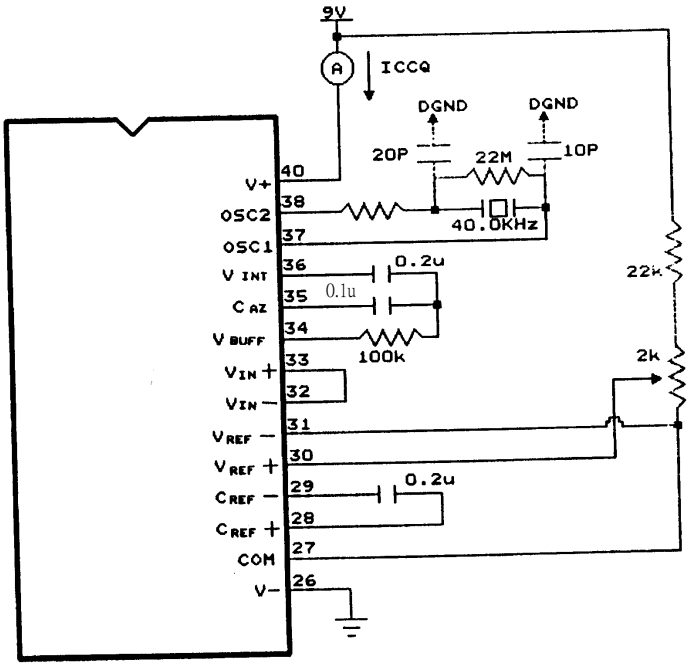


Fig.4 ICCQ Test Circuit

10．ERAL THEORY OF OPERATION

10.1 Analog Section :

In addition to the basic integrate and deintegrate dual slope phases discussed above, the ES5120 design incorporates an "Auto Zero" phase. The additional phase ensure that the integrator starts at zero volts (even after a severe over-range conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases :

(1) Auto Zero Phase

(2) Signal Integrate Phase

(3) Reference Deintegrate Phase

(4) ADC SYSTEM Timing

(1) Auto Zero Phase

During the Auto Zero phase, the differential input signal is disconnected from the measurement circuit by opening internal analog switches and the internal nodes are shorted to Analog Common (0 volt ref.) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit

comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle.

The Auto Zero phase residual is typically 10 to 15 μ A.

(2) Signal Integration Phase

Upon completion of the Auto Zero phase, the Auto Zero loop is opened and the internal differential inputs connect to V_{IN}^{+} and V_{IN}^{-}. The differential input signal is then integrated for a fixed time period, which in the ES5120 is 2000 counts (4000 clock periods). The externally set clock frequency is divided by two before clocking the internal counters. The integration time period is :

$$T_{INT} = \frac{4000}{fosc} = 2000 \text{ Counts}$$

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common as in battery powered applications, V_{IN}- should be tied to Analog Common.

Polarity is determined at the end of signal integration phase. The sign bit is a "true polarity" indication in that signals less than 1 LSB are correctly determined. This allows precision null detection which is limited only by device noise and Auto Zero residual offsets.

(3) Reference Integrate (Deintegrate) Phase

The reference capacitor, which was charged during the Auto Zero phase, is connected to the input of the integrating amplifier. The internal sign logic ensures that the polarity of the reference voltage is always connected in the phase which is opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate which is determined by the reference potential.

The amount of time required (T_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration phase :

$$T_{DEINT} = \frac{R_{INT}\ C_{INT}\ V_{INT}}{V_{REF}}$$

The digital reading displayed is :

$$\text{Digital Count} = 2000\frac{V_{IN+}\ V_{IN-}}{V_{REF}}$$

(4) ADC System Timing

The oscillator frequency is divided by 2 prior to clocking the internal decade counters. Each phase of the measurement cycle has the following length :

Auto Zero : 1999 to 5999 counts

Signal Integrate : 2000 counts

Deintegrate : 1 to 4001 counts

10.2 Frequency counter theory of Operation :

In addition to serving as an analog to digital converter, the ES5120 internal counter can also function as a frequency counter, (Figure 5). In the counter mode,

pulses at the RANGE/FREQ input will be counted and displayed.

The ES5120 frequency counter derives its timebase from the colck oscillator. The counter time base is :

$$T_{counter} = \frac{4,000,000}{F_{osc}}$$

Thus, the counter will operate with a 1 second timebase when a 40 kHz oscillator is used. The frequency counter accuracy is determined by the oscillator

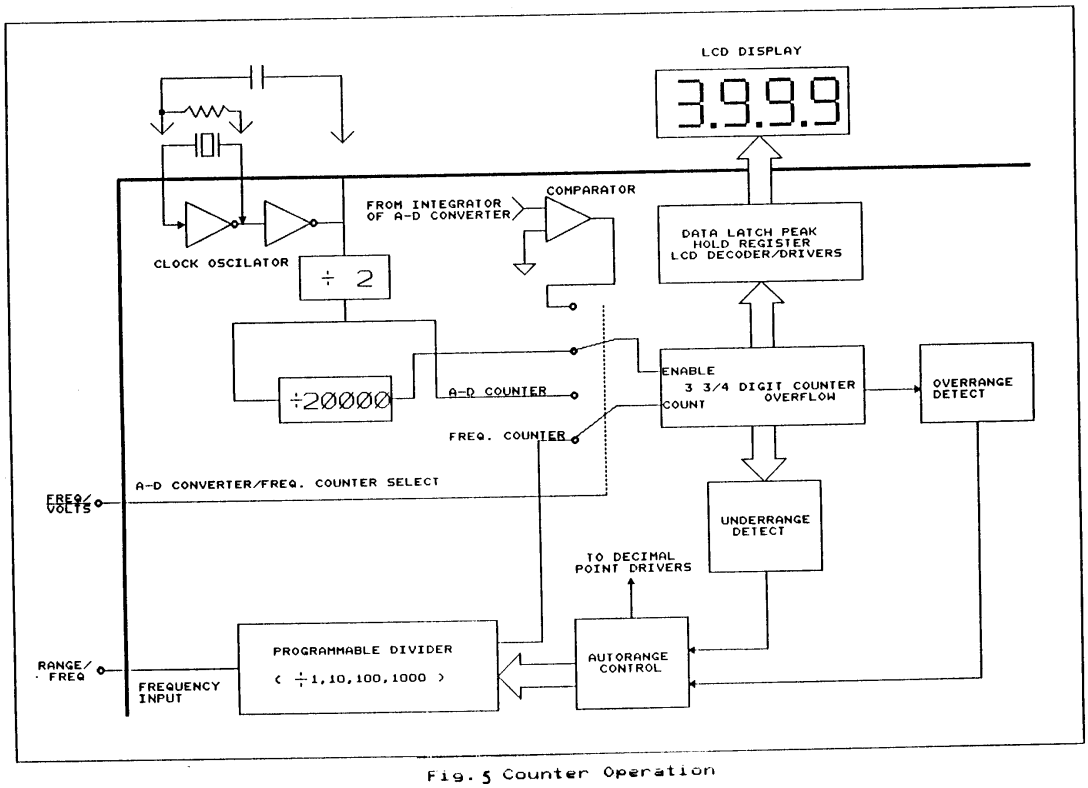


Fig. 5 Counter Operation

accuracy. For accurate frequency measurements, a crystal oscillator is recommended.

The frequency counter will automatically select the proper range. Autorange operation extends over four decades, from 3.999 kHz to 3.999 MHz. Decimal points are set automatically in the frequency mode, (Figure 6).

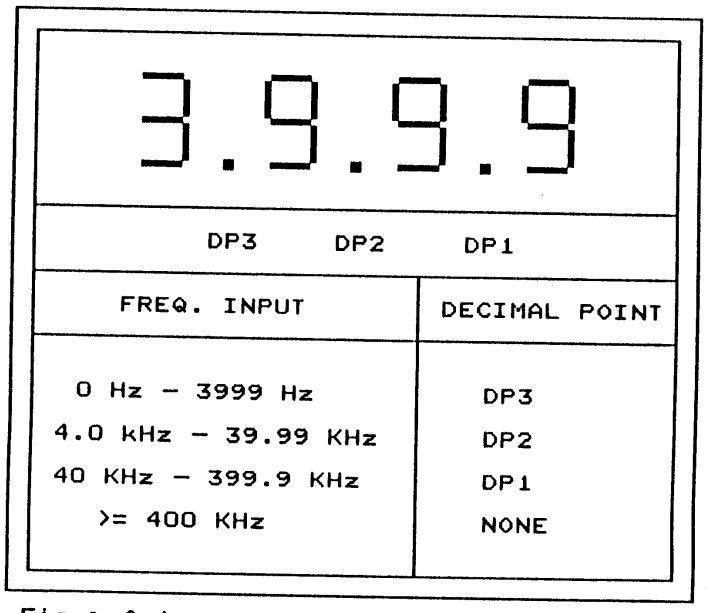


Fig.6 Autorange Decimal Point Seclction
Frequency Counter Input

The logic switching levels of the RANGE/FREQ input are CMOS levels. For best counter operation, an external buffer is recommended.

10.3 Logic Probe Theory of Operation :

This mode is selected when the LOGIC input is high. Two dual purpose pins, which normally control the decimal points, are used as logic inputs. Connecting either input to a logic high level will turn on the corresponding LCD annunciator, Also when the "low" annunciator is on the buzzer will be on. As with the Frequency Counter input, external level shifters/buffers are recommended for the logic probe inputs. (Fig.7)

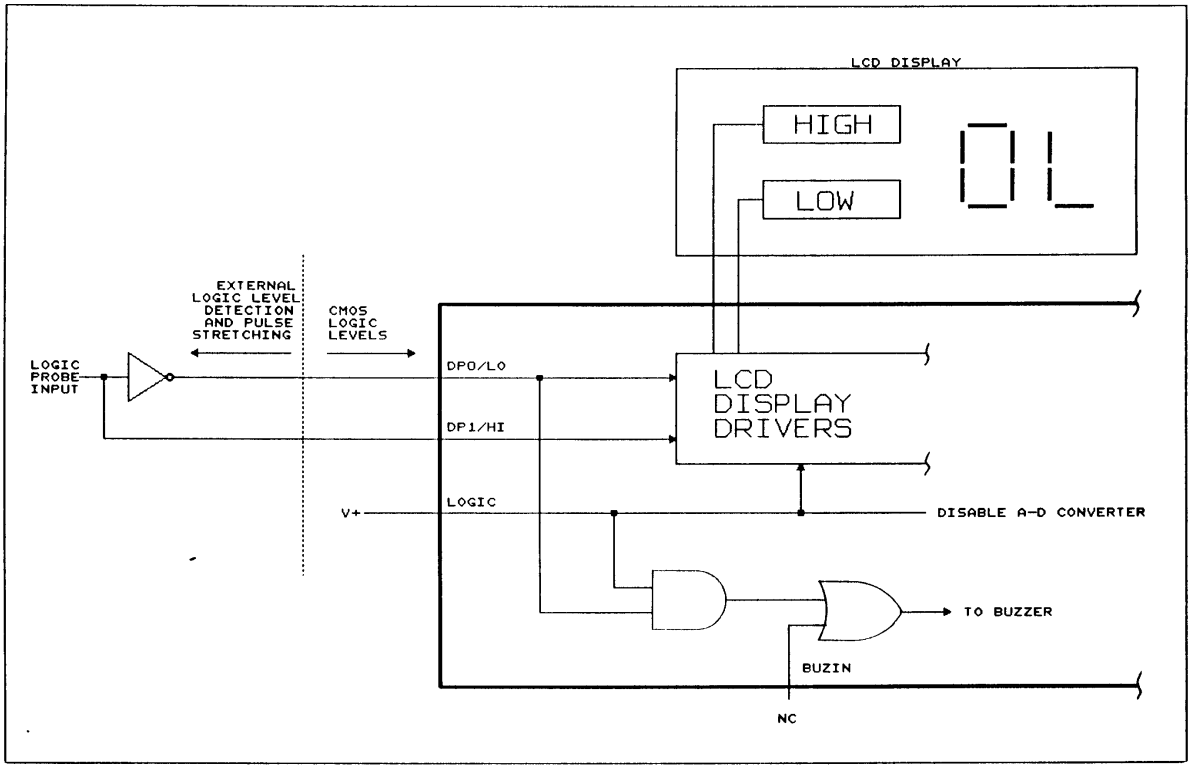


Fig. 7 Logic Simplified Schematic and Its Corresponing LCD Display

When the logic probe function is selected while FREQ/VOLTS is low (A/D mode). the analog to digital converter will remain in the autozero mode. The LCD display will read "OL" and all decimal points will be off. (Fig. 6 - Display)

If the logic probe is active while FREQ/VOLTS is high (counter mode) the frequency counter will continue to operate. The display will read "OL" but the decimal points will be visible. If the logic probe input is also connected to the RANGE/FREQ input, then bringing the LOGIC input low will immediately display the frequency at the logic probe input.

10.4 Selection of operating Mode

The operating modes are selected with the functional control inputs. The control input truth table is shown in Table 1.

Table 1. Control Input Truth Table

Logic Input			Function
FREQ/VOLTS	RANGE/FREQ	LOGIC	
×	×	1	Logic Probe
○	○	○	A/D Converter,Vfullscale=2*V_{REF}
○	1	○	A/D Converter,Vfullscale=20*V_{REF}
1	Freguency Counter Input	○	Frequency Counter

Note = Logic "0" = DGND

Logic "1" = V+

10.5 LCD Display

The ES5120 drives a triplex (multiplexed 3:1) liquid crystal display with three backplanes. The LCD display can include decimal points, polarity sign, and annuciators for overrange, peak hold, high and low logic levels, and low battery Fig. 8 shows the assignment of the display segments to the backplanes and the segment drive lines. The back plane drive frequency is obtained by dividing the oscillator frequency by 240.

40-pin DIP Pin No	44-pin QFP Pin No	BP1	BP2	BP3
1	40	Low	〝—〞	E4
2	41	A4	G4	D4
3	42	B4	C4	DP3
4	43	HIGH	F3	E3
5	44	A3	G3	D3
6	1	B3	C3	DP2
7	2	OVER	F2	E2
8	3	A2	G2	D2
9	4	B2	C2	DP1
10	5	PEAK	F1	E1
11	6	A1	G1	D1
12	7	B1	C1	BATT
13	8			BP3
14	9		BP2	
15	10	BP1		

Fig. 8 LCD Backplane and Segment Assignments

Backplane waveform are shown in Fig. 9. These appear on output BP1, BP2, and BP3. They remain the same regardless of the segments being driving.

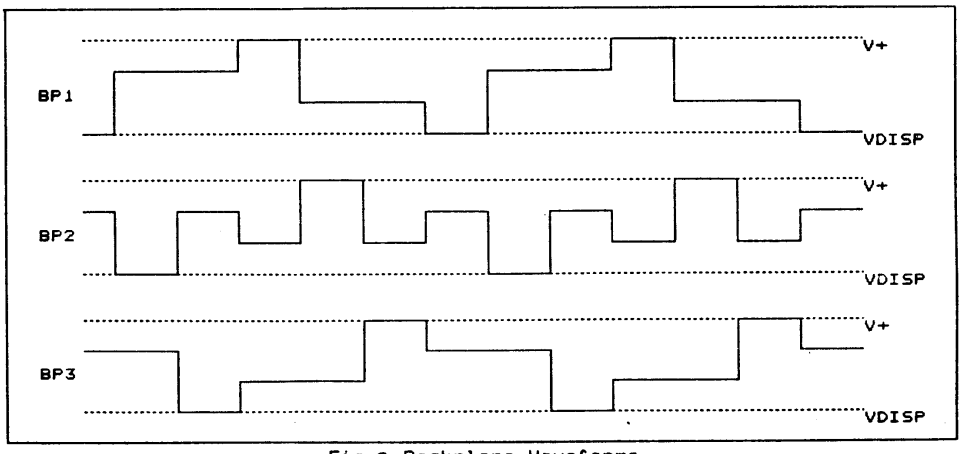


Fig.9 Backplane Waveforms

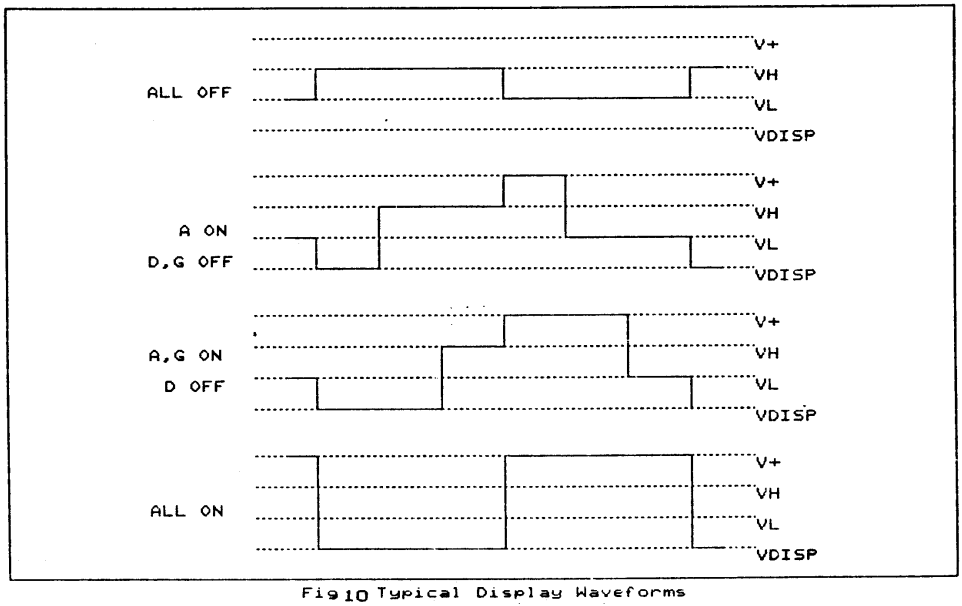
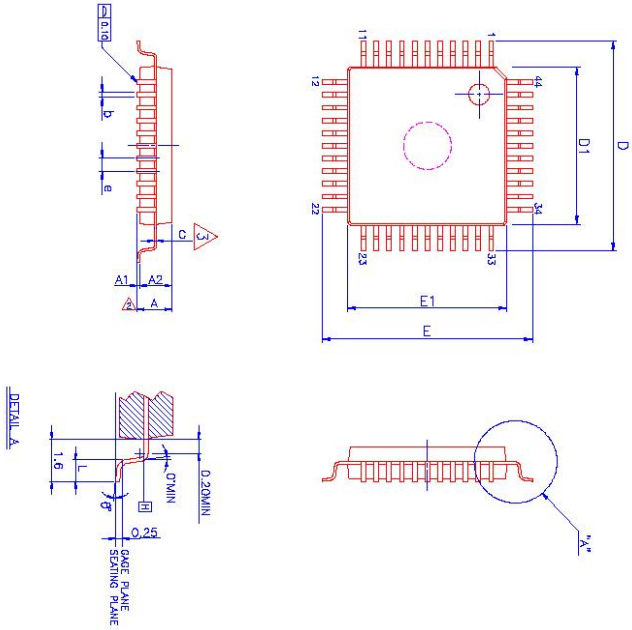


Fig.10 Typical Display Waveforms

Other display output lines have waveforms that vary depending on the displays values. Fig. 10 shows a set of waveforms for the AGD outputs of one digit for several combinations of "ON" segments.

１１．包裝(Package)

44-pin QFP package



	SYMBOLS	MIN.	NOM	MAX.
	A	—	—	2.7
	A1	0.25	0.30	0.35
3	A2	1.9	2.0	2.2
	b		0.3 (TYP.)	
	D	13.00	13.20	13.40
	D1	9.9	10.00	10.10
	E	13.00	13.20	13.40
	E1	9.9	10.00	10.10
	L	0.73	0.88	0.93
	e		0.80 (TYP.)	
3	θ°	0	—	7
	C	0.1	0.15	0.2

UNIT : mm

NOTES:

1. JEDEC OUTLINE:MO－108 AA－1
2. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

40-pin DIP package

	MILLIMETERS	
DIM	MIN	MAX
A	50.29	51.82
B	15.49	16.00
C	3.81	5.08
D	0.41	0.51
F	1.27 TYP	
G	2.54 BASIC	
H	0.76	1.78
J	0.23	0.30
K	3.94	4.95
L	15.24 BASIC	
N	1.02	1.52