承永資訊科技
CYRUSTEK CO.

ES5117 3 1/2 DVM with LED Display and Hold

Features

- Guaranteed zero reading with zero input
- Low input leakage current (1pA typical)
- Internal reference with low temperature drift (60***ppm/℃*** typically)
- Low noise (15uVp-p typical)
- **Direct LED display driver**
- Differential input and voltage reference
- Precise null detection with true polarity at zero
- Internal clock circuit
- No additional active circuits required
- **Display Hold**

Description

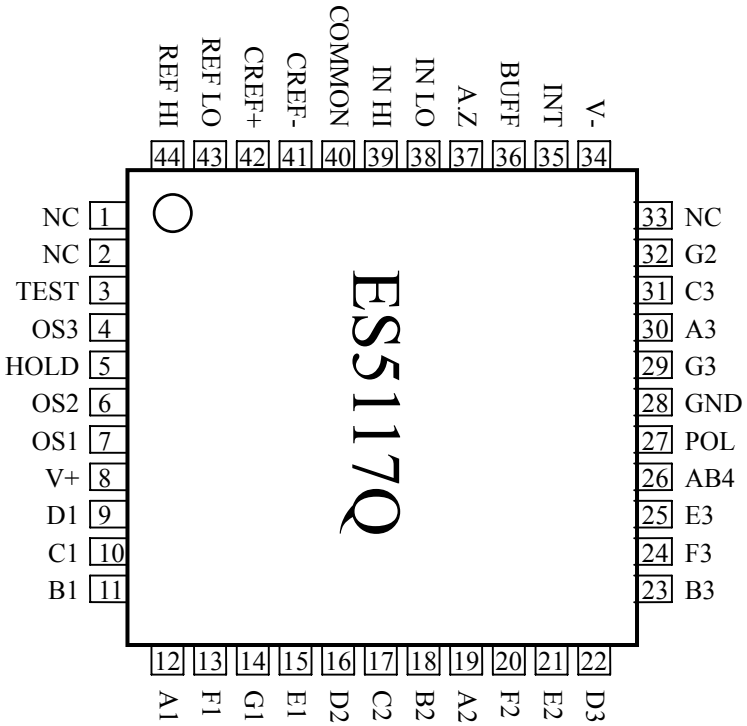
The ES5117 is a monolithic CMOS 3 1/2 digit **LED display** A/D converter with **Display Hold** function. It contains the internal clock, voltage reference, seven-segment decoder and LED display driver. The improved internal zener reference voltage circuit gives the analog common a small temperature coefficient of 60***ppm/℃*** typically. The high accuracy characteristics of the ES5117 perform very low linearity error and rollover error. The high input impedance (>$10^{12}\Omega$) and low input leakage current (1pA typical) give the ES5117 a good application in the field of high impedance circuit measurement. The differential input and reference are suitable for measuring bridge transducer or ohms by using ratio-metric method. The dual slope conversion technique makes the ES5117 a good normal and common mode rejection ratio. With a suitable oscillator frequency, the ES5117 has a high rejection of 50Hz, 60Hz and 400Hz line frequency noise. With single power supply, a few passive components and a LED display, ES5117 can be built as high performance panel meter.

Application

Digital panel meters

Pin Assignment

QFP-44pin package



Pin Description

Pin No	Symbol	Type	Description
1	NC	-	No connected.
2	NC	-	No connected.
3	TEST	I	Pull high to V+ all segments will be activated.
4	OS3	-	Crystal oscillator connection.
5	HOLD	I	Hold pin, pull high to hold display
6	OS2	-	Crystal oscillator connection
7	OS1	-	Crystal oscillator connection
8	V+	-	Positive supply voltage.
9	D1	O	LED segment line.
10	C1	O	LED segment line.
11	B1	O	LED segment line.
12	A1	O	LED segment line.
13	F1	O	LED segment line.
14	G1	O	LED segment line.
15	E1	O	LED segment line.
16	D2	O	LED segment line.
17	C2	O	LED segment line.
18	B2	O	LED segment line.
19	A2	O	LED segment line.
20	F2	O	LED segment line.
21	E2	O	LED segment line.
22	D3	O	LED segment line.
23	B3	O	LED segment line.
24	F3	O	LED segment line.
25	E3	O	LED segment line.
26	AB4	O	LED segment line.
27	POL	O	LED segment line.
28	GND	-	Power Ground
29	G3	O	LED segment line.
30	A3	O	LED segment line.
31	C3	O	LED segment line.
32	G2	O	LED segment line.
33	NC	-	No connected.
34	V-	-	Negative supply voltage.
35	INT	O	Integration cycle output.
36	BUFF	O	Integration resistor connection for buffer output.
37	A.Z	-	Auto-zero capacitor connection.
38	IN LO	-	Low analog input signal connection.
39	IN HI	-	High analog input signal connection.
40	COMMON	-	Set the common-mode voltage for the system.
41	CREF-	-	Negative capacitor connection for on-chip DC-DC converter.
42	CREF+	-	Positive capacitor connection for on-chip DC-DC converter.
43	REF LO	I	Low differential reference input connection.
44	REF HI	I	High differential reference input connection.

Absolute Maximum Ratings

Characteristic	Rating
Supply Voltage V+ V-	+6V -6V
Analog Input Voltage (either input)	V+ to V-
Reference input voltage (either input)	V+ to V-
Clock input	GND to V+
Power Dissipation. Flat Package	800mW
Operating Temperature	0℃ to 70℃
Storage Temperature	-65℃ to 160℃
Lead Temperature (Soldering, 10sec)	270℃

Electrical Characteristics

Parameter	Symbol	Test Condition		Min.	Typ.	Max	Units
Power Supply	V+	With respect to GND		+4	+5	+6	V
	V-			-4	-5	-6	
Zero Input Reading	-	V_{IN} = 0V , Full-Scale=200.0mV		-000.0	± 000.0	+000.0	Digital Reading
Ratio-metric Reading	-	$V_{IN}=V_{REF}$, V_{REF}=100.0mV		999	999/1000	1000	Digital Reading
Linearity (Max. deviation form best straight line fit)	-	Full-Scale=200mV or Full-Scale=2.000V		-1	± 0.2	+1	Counts
Roll-over Error	-	$-V_{IN} = +V_{IN}$ ~ 200.0mV		-1	± 0.2	+1	Counts
Common Mode Rejection Ratio	-	V_{CM}=± 1V, V_{IN}=0V Full-Scale=200.0mV		-	50	-	uV/V
Noise	-	V_{IN} = 0V , Full-Scale=200.0mV		-	15	-	uVp-p
Input leakage current	-	V_{IN} = 0V		-	1	10	pA
Zero Reading Drift	-	V_{IN}=0V , 0℃ <= T_A <= 70℃		-	0.2	1	uV/℃
Analog COMMON Voltage (with respect to V+)	-	25K Ω Between Common and Positive Supply		2.8	3.0	3.2	V
Analog COMMON Temperature Coefficient	-	25K Ω Between Common and V+ , 0℃ <= T_A <= 70℃		-	60	75	ppm/℃
Supply Current (Does not include LED drive current and COMMON current)	-	V_{IN}=0V		-	0.6	0.75	mA
Segment Sinking Current		V+ = 5.0V, Segment Voltage=3V	Except pin26	5	8		mA
			pin26 only	10	16		

Function Description

1. Analog Common

The COMMON pin is used to set the common-mode voltage for the system which the input signals are floating. In most of the applications, IN LO, REF LO and COMMON pins are usually connected. It can remove common-mode voltage concerns. In other applications, INLO does not connect with COMMON. The ES5117 generates a common mode voltage, which has the high CMRR (86dB typical). Nevertheless, it should be care to prevent the output of the integrator form saturation.

The COMMON pin is also used as a voltage reference. It outputs a voltage, which is around 2.9 volts below the positive supply. The COMMON voltage has a low output impedance of 15Ω typically.

The analog COMMON is connected internally to a NMOS, which can sink 30mA. This NMOS will hold the COMMON voltage at 2.9 volts when an external load attempts to pull the COMMON voltage toward the positive supply. The source current of COMMON is only 10uA, so it is easy to pull COMMON voltage to a more negative voltage.

When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low temperature coefficient less than 60ppm/℃ typically. The voltage can be used to generate the reference voltage.

2. Reference Voltage

For a 1000 counts reading, the input signal must be equal to the reference voltage. As a result, it requires the input signal be twice the reference voltage for a 2000 counts full-scale reading. Thus, for the 200.0mV and 2.000V full-scale, the reference voltage should equal 100.0mV and 1.000V. In some applications the full-scale input voltage may be different to 200mV or 2.000V. For example, in the 600mV full-scale applications, the reference voltage should be set to 300mV.

The differential reference should be used during the measurement of resistor by the ratio-metric method and when a digital reading of zero is desired for Vin≠0, a compensating offset voltage can be applied between COMMON and IN LO, and the voltage of being measured is connected between COMMON and IN HI.

3. System Timing

The oscillator frequency is divided by four prior to clocking the internal decade counters. The signal integration takes a fixed 1000 counts time period which is equal to 4000 clock pulse. The back plane drive signal is derived by dividing oscillator frequency by 800. To make a maximum noise rejection of line frequency(60Hz or 50Hz), the signal integration period should be a multiple of the line frequency period. For 60Hz-noise rejection, oscillator frequencies of 120KHz, 80KHz, 60KHz, 48KHz, 40KHz, etc. should be selected. For 50Hz-noise rejection, oscillator frequencies of 100KHz, 50KHz 40KHz, etc. would be suitable.

For all rages of frequency Rosc should be 100KΩ, Cosc is selected form the approximate equation f~0.45/RC. For 48KHz clock (3reading/second), Cosc=100pF.

4. Integrating Resistor

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 100uA. Both of them can supply 20uA drive currents with negligible linearity errors. The integrating resistor is chosen to remain linear drive region in the output stage. It should not be so large that the leakage current of printed circuit board will induce errors. The recommended integrating resistor value for the 200mV and 2V full-scale are 47KΩ and 470KΩ respectively.

5. Integrating Capacitor

The integrating capacitor should be selected to maximize integrator output voltage swing without causing output saturation. For 3 readings/second (48KHz clock), a 0.22uF value of C_{INT} is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ± 2V integrator swing.

The integrating capacitor must have low dielectric absorption to minimize roll-over error. An inexpensive polypropylene capacitor is recommended.

6. Auto-Zero Capacitor

The auto-zero capacitor size has some influence on system noise. A 0.47uF capacitor is recommended for 200mV full scale. A 0.047uF capacitor is adequate for 2V full-scale range applications. A mylar type dielectric capacitor is adequate.

7. Reference Voltage Capacitor

The reference voltage used to ramp the integrator output voltage back to zero during the

reference integrate cycle is stored on C_{REF}. A 0.1uF value capacitor is acceptable when INLO is connected with COMMON. A mylar type dielectric capacitor is adequate.

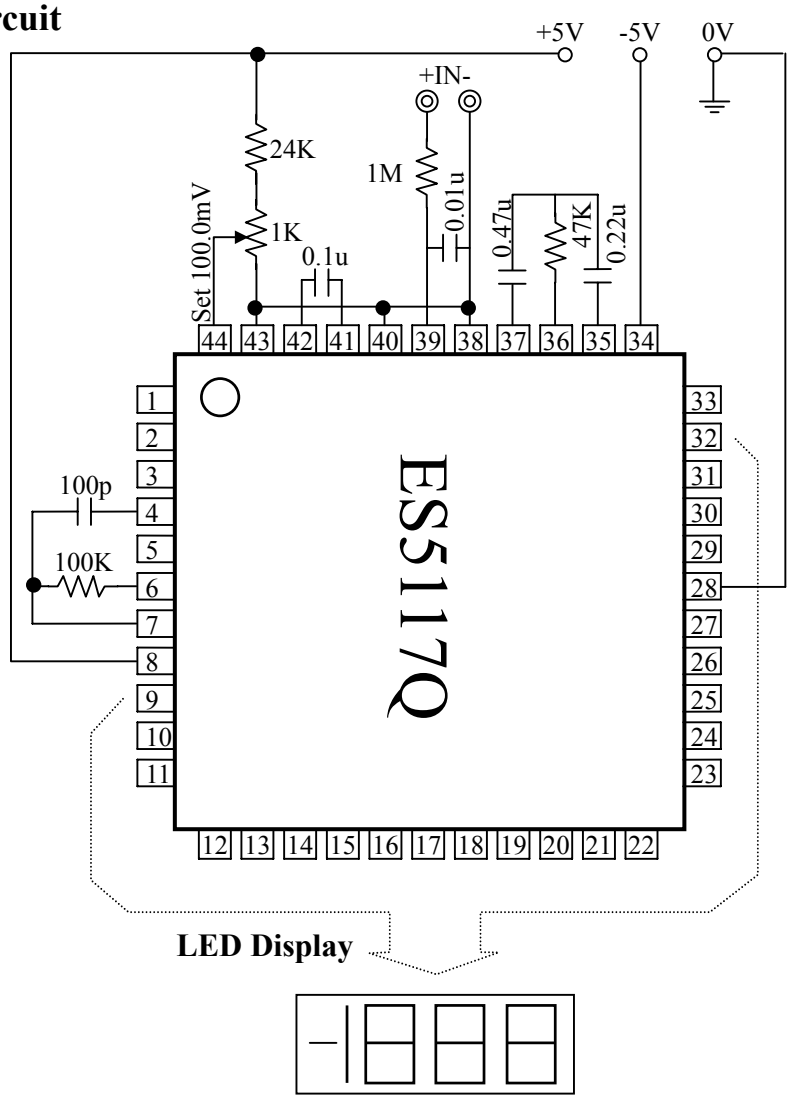
8. TEST

The TEST pin is tied to the negative logic supply through a 500Ω resistor. When TEST is pulled high to V+ all segments will be turned on and the display should read -1888.

9. Hold

When the hold pin is connected to V+ the conversion result will not be update. The conversion is still free running during hold mode.

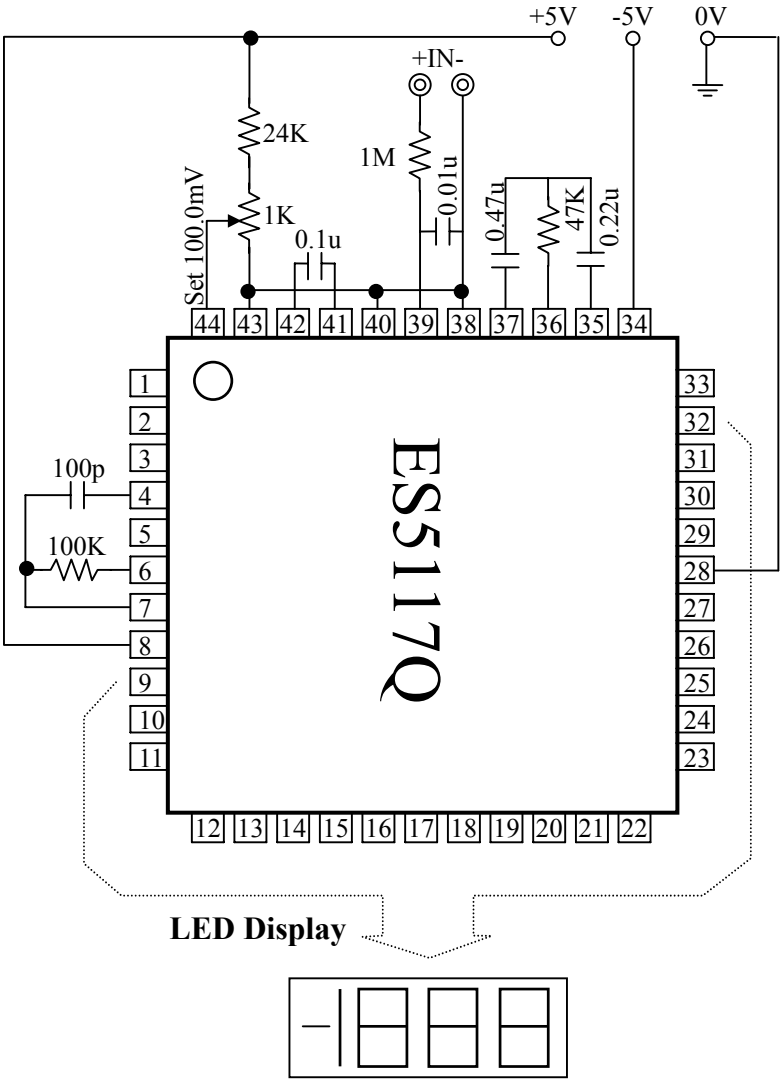
TEST Circuit



Clock Frequency 48KHz (3 readings/second)

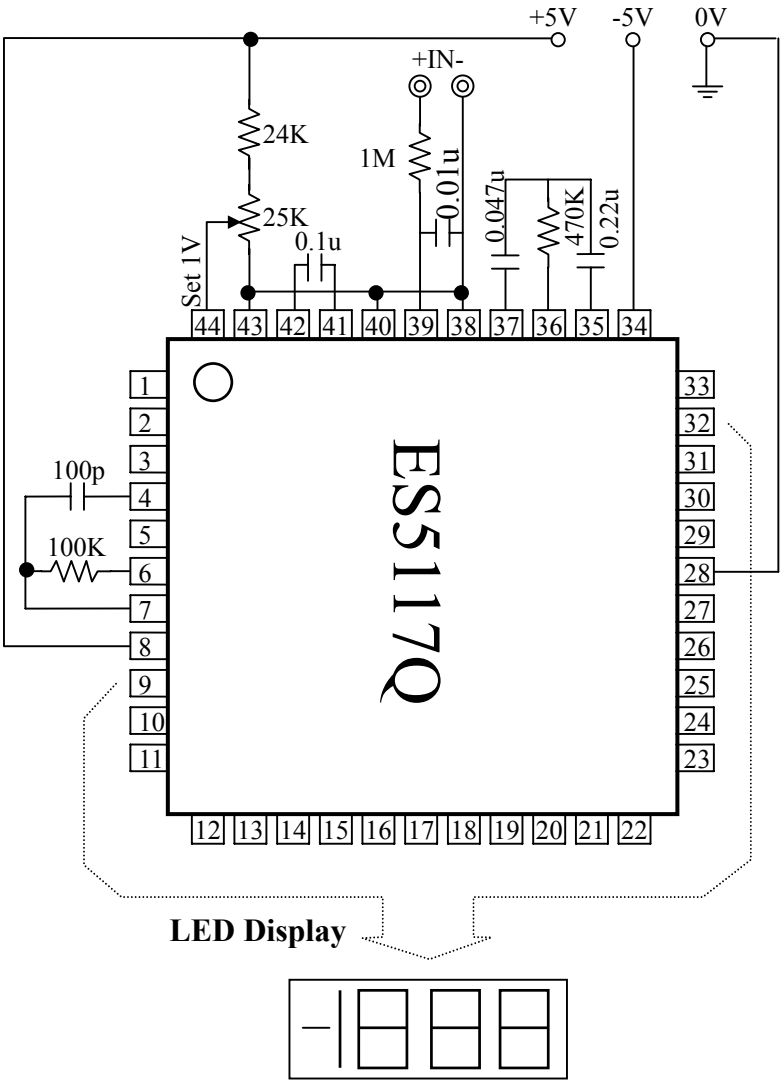
Application Circuit

1. This circuit uses analog COMMON voltage as reference voltages. Values here are for 200.0mV full scale, 3readings/second.



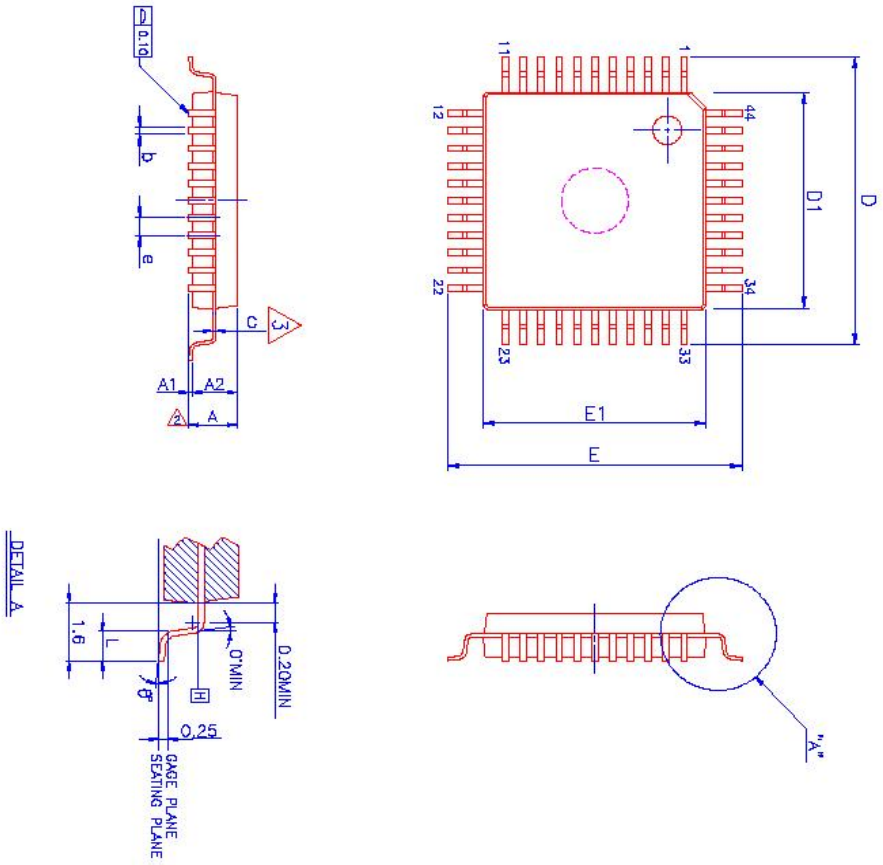
Clock Frequency 48KHz (3 readings/second)

2. The values of this circuit are for 2.000V full scale, 3 readings/second.



Clock Frequency 48KHz (3 readings/second)

Package Outline : 44-pin QFP



	SYMBOLS	MIN.	NOM	MAX.
	A	—	—	2.7
	A1	0.25	0.30	0.35
3	A2	1.9	2.0	2.2
	b		0.3 (TYP.)	
	D	13.00	13.20	13.40
	D1	9.9	10.00	10.10
	E	13.00	13.20	13.40
	E1	9.9	10.00	10.10
	L	0.73	0.88	0.93
	e		0.80 (TYP.)	
	θ°	0	—	7
3	C	0.1	0.15	0.2

UNIT : mm

NOTES:

1. JEDEC OUTLINE:MO-108 AA-1
2. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.