ES228(6000counts dual)

DMM Analog front end

Features

- 6000 counts dual ADC core (2.8-11 cnvs/s.)
- Input signal full scale: 630mV
- 100LQFP package
- ±3V DC regulated power supply
- Support digital multi-meter function.

  *Voltage measurement (AC/DC)

  *Current measurement (AC/DC)

  *Support AC+DC RMS mode

  *Dual mode for AC/DC voltage or current

  *Resistance measurement (0.00Ω – 300MΩ)

  *Conductance measurement (600nS)

  *Capacitance measurement (0.000nF –300mF)
  (Taiwan patent no.: 323347, 453443)

  (China patent no.: 200710106702.8)

  *Diode or continuity mode measurement

  *Frequency counter with duty cycle display:

  1.00Hz – 60.00MHz

  5.0% – 95.0%
- User-defined ADP mode (8 input channels).
- Support Peak-hold mode
- Built-in Inrush indicator circuit.
- Hazard voltage indication for R/C/D/F modes
  (**Taiwan patent no.: 536023**)
  (**China patent no.:ZL 2013 1 0453561.2**)
- 3dB BW selectable for low pass filter (dual) at AC mode
  (**Taiwan patent no.: 362409**)
  (**China patent no.: 200920156001.X**)
- Band-gap reference voltage output
- 3-wire serial bus for MPU I/O port
- MPU I/O power level selectable by external pins
- On-chip buzzer driver
- Multi-level battery voltage detection
- Support sleep mode by external chip select pin

Application

Clamp-on meter

Digital multi-meter

Description

ES228 is an analog frond end chip of DMM built-in dual 6000 counts dual-slope ADCs. The dual ADC cores are fully operated individually. ES228 provides voltage & current (AC/DC) measurement, resistance measurement, capacitance measurement, diode/continuity measurement, frequency measurement and duty cycle measurement. ES228 also supports multi-level battery detection, low-pass-filter, and dual mode measurement for ACV+DCV, ACA+DCA, DCV&DCA, ACV&ACA. A 3-wire serial bus for MPU I/O port will be used easily for firmware design. Flexible function design is supported for different kinds of DMM or Clamp-on meter application.

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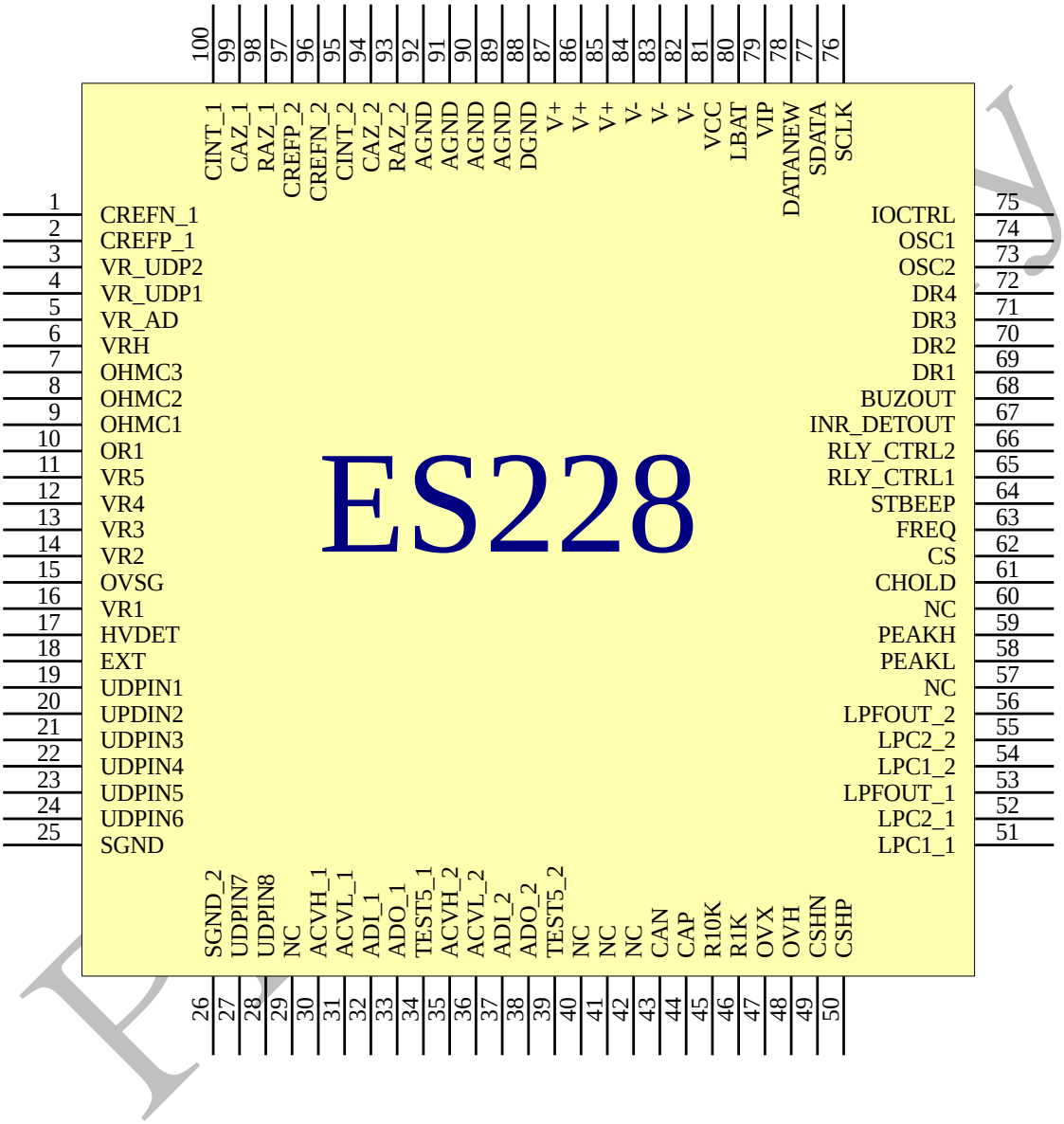
Pin Assignment



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Pin Description

Pin No	Symbol	Type	Description
1	CREFN_1	O	Negative connection for reference capacitor of ADC1.
2	CREFP_1	O	Positive connection for reference capacitor of ADC1.
3	VR_UDP2	I	Reference input voltage in UDP2 mode. Typically 200mV (VRH-VR_UDP2)
4	VR_UDP1	I	Reference input voltage in UDP1 mode. Typically 200mV (VRH-VR_UDP1)
5	VR_AD	I	Reference input voltage in ADC mode. Typically 200mV (VRH-VR_AD)
6	VRH	O	Output of band-gap voltage reference. Typically –1.23V
7-9	OHMC1-3	O	Filter capacitor connection1-3 for resistance mode.
10	OR1	O	Reference resistor connection for 600.00Ω range
11	VR5	O	Voltage measurement ÷9999 attenuator (1000.0V)
12	VR4	O	Voltage measurement ÷1000 attenuator (600.00V)
13	VR3	O	Voltage measurement ÷100 attenuator (60.000V)
14	VR2	O	Voltage measurement ÷10 attenuator (6.0000V)
15	OVSG	O	Sense low voltage for resistance/voltage measurement
16	VR1	I	Measurement Input. Connect to a precise 10MΩ resistor.
17	HVDET	I	Connect to AGND
18	EXT	I	When SGND2TOEXT is set, the signal ground of ADC2 is switched from SGND2 to EXT
19	UDPIN1	I	UDP1 mode input terminal1.
20	UDPIN2	I	UDP2 mode input terminal2.
21	UDPIN3	I	UDP3 mode input terminal3.
22	UDPIN4	I	UDP4 mode input terminal4.
23	UDPIN5	I	UDP5 mode input terminal5.
24	UDPIN6	I	UDP6 mode input terminal6.
25	SGND1	I/G	Signal ground for ADC1.
26	SGND2	I/G	Signal ground for ADC2.
27	UDPIN7	I	UDP7 mode input terminal7.
28	UDPIN8	I	UDP8 mode input terminal8.
29	NC	-	No connection.
30	ACVH_1	I	DC signal high input in ADC1_AC mode. Connect to positive output of external AC to DC converter.
31	ACVL_1	I	DC signal low input in ADC1_AC mode. Connect to negative output of external AC to DC converter.
32	ADI_1	I	Negative input of internal AC to DC OP Amp for ADC1_AC mode.
33	ADO_1	O	Output of internal AC to DC OP Amp for ADC1_AC mode.
34	TEST5_1	O	Buffer output of SGND1 or frequency output for ADC1_AC mode.
35	ACVH_2	I	DC signal high input in ADC2_AC mode. Connect to positive output of external AC to DC converter.
36	ACVL_2	I	DC signal low input in ADC2_AC mode. Connect to negative output of external AC to DC converter.
37	ADI_2	I	Negative input of internal AC to DC OP Amp for ADC2_AC mode.
38	ADO_2	O	Output of internal AC to DC OP Amp for ADC2_AC mode.
39	TEST5_2	O	Buffer output of SGND2 or frequency output for ADC2_AC mode.
40	NC	-	No connection.
41	NC	-	No connection.
42	NC	-	No connection.
43-44	CA-/CA+	O	Auto-zero capacitor connection for capacitor measurement
45	R10K	O	Connect to a precise 10KΩ resister for capacitor measurement.
46	R1K	O	Connect to a precise 1KΩ resister for capacitor measurement.
47	OVX	I	Sense input for resistance/capacitance measurement
48	OVH	O	Output connection for resistance measurement

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49-50	CSH-/CSH+	O	Capacitor connection for inrush mode
51	LPC1_1	O	Capacitor C1 connection for internal low-pass filter of ADC1
52	LPC2_1	O	Capacitor C2 connection for internal low-pass filter of ADC1
53	LPCOUT_1	O	Capacitor C1 connection for internal low-pass filter of ADC1
54	LPC1_2	O	Capacitor C1 connection for internal low-pass filter of ADC2
55	LPC2_2	O	Capacitor C2 connection for internal low-pass filter of ADC2
56	LPCOUT_2	O	Capacitor C1 connection for internal low-pass filter of ADC2
57	NC	-	No connection.
58	PEAKL	O	Minimum peak hold output
59	PEAKH	O	Maximum peak hold output.
60	NC	-	No connection.
61	CHOLD	I	Bypass capacitor for peak mode
62	CS	I	Chip selection input.
63	FREQ	I	Frequency counter input, offset V-/2 internally by the chip.
64	STBEEP	O	Fast low-impedance when sensed output for CONT./Diode mode
65	RLY_CTRL1	O	No connection.
66	RLY_CTRL2	O	No connection.
67	INR_DETOUT	O	Output logic high (VCC) level when detect inrush signal.
68	BUZOUT	O	Buzzer output driver
69	DR1	O	Open drain output 1. (VCC-IOCTRL)
70	DR2	O	Open drain output 2. (VCC-IOCTRL)
71	DR3	O	Open drain output 3. (VCC-IOCTRL). Or it is used to output the period of signal from VR1 when .
72	DR4	O	Open drain output 4. (VCC-IOCTRL). Or it is used to output the period of signal from UDP.
73-74	OSC1/OSC2	-	4MHz crystal oscillator connection
75	IOCTRL	I	MCU I/O logic low level setting
76	SCLK	I	MCU serial clock input
77	SDATA	I/O	MCU serial data input
78	DATANEW	O	Data ready output.
79	VIP	-	No connection
80	LBAT	I	Multi-level low battery configuration input. Simple external resistor divider is required.
81	VCC	P	MCU power connection
82-84	V-	P	Negative supply voltage.
85-87	V+	P	Positive supply voltage.
88	DGND	G	Digital ground.
89-92	AGND	G	Analog ground.
93	RAZ_2	O	Buffer output pin in AZ and ZI phase for ADC2.
94	CAZ_2	O	Auto-zero capacitor connection for ADC2.
95	CINT_2	O	Integrator output for ADC2. Connect to integral capacitor.
96	CREFN_2	O	Negative connection for reference capacitor of ADC2.
97	CREFP_2	O	Positive connection for reference capacitor of ADC2.
98	RAZ_1	O	Buffer output pin in AZ and ZI phase for ADC1.
99	CAZ_1	O	Auto-zero capacitor connection for ADC1.
100	CINT_1	O	Integrator output for ADC1. Connect to integral capacitor.

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Absolute Maximum Ratings

Characteristic	Rating
Supply Voltage (V- to AGND)	-4V
Supply Voltage (V+to AGND)	+4V
Analog Input Voltage & EXTSRC pin	V- -0.6 to V+ +0.6
V+	V+ ≥ (AGND/DGND+0.5V)
AGND/DGND	AGND/DGND ≥ (V- -0.5V)
Digital Input (IOCTRL=V-)	V- -0.6 to VCC+0.6
Power Dissipation. Flat Package	500mW
Operating Temperature	-20℃ to 70℃
Storage Temperature	-55℃ to 125℃

Electrical Characteristics

TA=25℃, V- = -3.0V

Parameter	Symbol	Test Condition	Min.	Typ.	Max	Units
Power supply	V+, V-		±2.8	±3.0	±3.2	V
Operating supply current In DCV&DCA mode	I_{DD}	Normal operation	—	2.6	—	mA
	I_{SS}	In sleep mode	—	25	—	μA
ADC Voltage roll-over error		10MΩ input resistor	—	—	±0.1	%F.S[1]
ADC voltage nonlinearity	NLV1	Best case straight line	—	—	±0.02	%F.S[1]
Voltage full scale range of ADC		VRH-VR_AD= 200mV	—	600	630	mV
Input Leakage for VR1 input			-10	1	10	pA
Zero input reading		10MΩ input resistor	-000	000	+000	Count
Band-gap reference voltage	V_{RH}	100KΩ resistor between VRH and AGND	-1.30	-1.22	-1.14	V
Internal pull-high to 0V current		Between V- pin and CS	—	1.2	—	μA
AC frequency response at 6.000V range		±1%	—	60-600	—	HZ
		±5%	—	600-6000	—	
3dB frequency for LPF[2] active	f_{3dB}	3dB=Full (ADP)	70	—	—	kHz
		3dB=10k (ADP)	—	10	—	kHz
		3dB=1k (ADP)	—	1	—	kHz
Multi-level low battery detector	V_{t1}	LBAT vs. V-	—	2.29	—	V
	V_{t2}		—	2.12	—	V
	V_{t3}		—	1.91	—	V
Peak-hold mode pulse width		ACIN =40 ~ 400Hz	—	1000	—	us
STBEEP comparator in Diode mode		OVX to SGND	—	+9	—	mV
STBEEP comparator in Cont. mode		OVX to SGND	—	-7	—	mV

[1] Full Scale (6000 counts for ADC)

[2] ES228 built-in 2nd order low pass filter available for AC mode

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Inrush triggered delay time		50Hz square wave		1.1		ms
Inrush triggered level		UDPn to SGND. 50Hz square wave.		37		mVpp
Frequency input sensitivity (*FREQ*)	Fin	Square wave with Duty cycle 40-60%	500	—	—	mVp
Frequency input sensitivity (*FREQ*)	Fin	Sine wave	400	—	—	mVrms
Reference voltage temperature coefficient	TC_{RF}	100KΩ resister Between VRH -20℃<TA<70℃	—	50	—	ppm/℃
Capacitance measurement Accuracy		6nF – 300mF	-2.5	—	2.5	%F.S
			-30	—	30	counts

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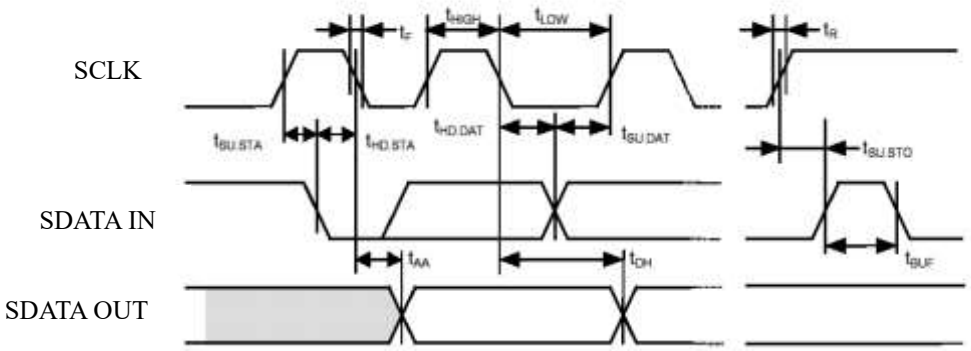
SIO electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCLK clock frequency	f_{SCLK}	-	-	100	kHz
SCLK clock time "L"	t_{LOW}	4.7	-	-	us
SLCK clock time "H"	t_{HIGH}	4.0	-	-	
SDATA output delay time	t_{AA}	0.1	-	3.5	
SDATA output hold time	t_{DH}	100	-	-	ns
Start condition setup time	$t_{SU.STA}$	4.7	-	-	us
Start condition hold time	$t_{HD.STA}$	4.0	-	-	
Data input setup time	$t_{SU.DAT}$	200	-	-	ns
Data input hold time	$t_{HD.DAT}$	0	-	-	
Stop condition setup time	$t_{SU.STO}$	4.7	-	-	us
SCLK/SDATA rising time	t_R	-	-	1.0	
SCLK/SDATA falling time	t_F	-	-	0.3	
Bus release time	t_{BUF}	4.7	-	-	

MPU I/O timing diagram



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Function Description

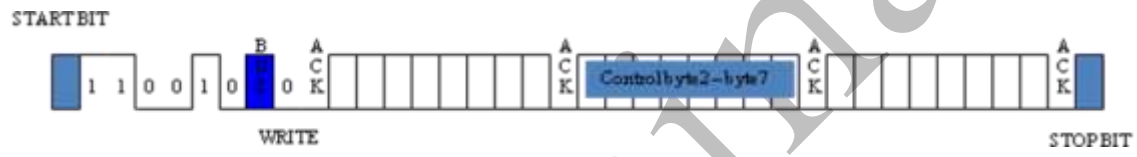
MPU serial I/O function overview

Introduction

ES228 configures a 3-wire serial I/O interface to external microprocessor unit (MPU). The SDATA pin is bi-directional and SCLK & DATANEW are unilateral. The SDATA pin is configured by open-drain circuit design. The DATANEW is used to check the data buffer of ADC ready or not. When the ADC conversion cycle is finished, the DATANEW pin will be pulled high until MPU send a valid read command to ES228. After the first ID byte is confirmed, the DATANEW will be driven to low until the next ADC conversion finished again. The data communication protocol is shown below. The write protocol is configured by an ID byte with nine command bytes. The read protocol is configured by an ID byte with sixteen data bytes.

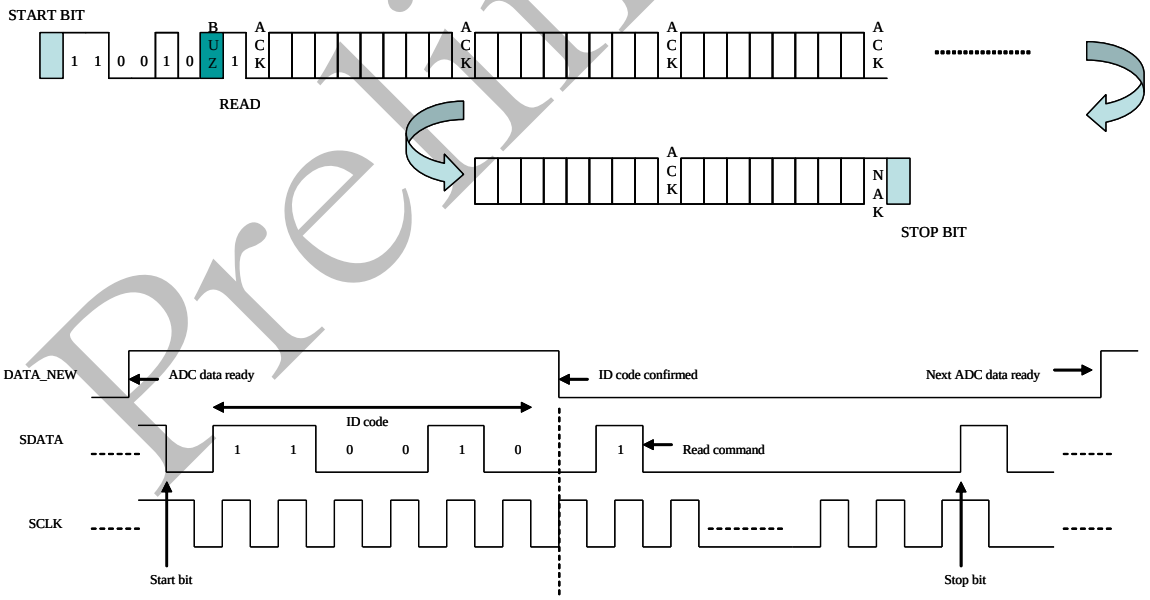
Write command:

ID byte, Write control byte1 ~ control byte9



Read command:

ID byte, Read data byte1, Read data byte1 ~ Read data byte16, Read data byte16



The ID byte of ES228 is header of “110010” followed by a buzzer on/off control bit and R/W bit. The start/stop bit definition is shown on the diagram below.

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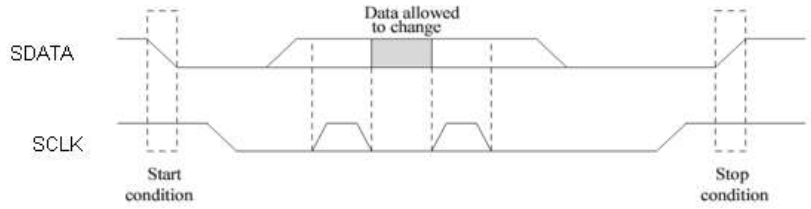
Start and Stop bit



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Read/Write command description

The write command includes one ID byte with four command bytes. If the valid write ID code is received by ES228 at any time, the write command operation will be enabled.

The next table shows the content of write command: (ADC1/ADC2 controlled individually)

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID	1	1	0	0	1	0	**BUZ**	**R/W=0**
W1	F3	F2	F1	F0	C1_AD1	C0_AD1	C1_AD2	C0_AD2
W2	AC_1	AC_2	Q2	Q1	Q0	B2	B1	B0
W3	VAHZ_1	VAHZ_2	FQ2_1	FQ1_1	FQ0_1	FQ2_2	FQ1_2	FQ0_2
W4	PCAL_1	PCAL_2	PEAK_1	PEAK_2	INA	FCOND	0	AD2OFF
W5	SUDP2_1	SUDP1_1	SUDP0_1	SUDP2_2	SUDP1_2	SUDP0_2	TMP24X_1	TMP24X_2
W6	LPF1_1	LPF0_1	LPF1_2	LPF0_2	VHZ1K_1	VHZ1K_2	PERDOUT	HRC
W7	SWAP	1	SHBP	DIOVSS	INTSEL	0	0	0
W8	0	0	1	1	DR1	DR2	DR3	DR4
W9	1	0	0	UDPX10_2	T1300_1	T1300_2	SGND2TOEXT	BYPASS

BUZ：Control bit for Buzzer

1：enable the driver to drive the buzzer.

0：disable the driver.

F3/F2/F1/F0：Measurement function control bit

F3	F2	F1	F0	Measurement mode	D0	D1	D2	D3	D4
0	0	0	0	DCV&ACV	DCV	ACV		V_Hz	INT
0	0	0	1	DCA&ACA	DCA	ACA		A_Hz	INT
0	0	1	1	VA dual	V	A	V_Hz	A_Hz	PHASE
0	1	1	1	Resistance mode	Res.	UDP			
1	0	0	0	Continuity Mode	Cont.	UDP			
1	0	0	1	Capacitance mode	Cap.	UDP			
1	0	1	0	Diode mode	Diode	UDP			
1	0	1	1	LED mode	LED	UDP			
1	1	0	0	Hz + duty mode	Hz		Duty	Hz/Duty	
1	1	0	1	UDP dual mode	UDP	UDP		Hz	

C1_AD1/C0_AD1/C1_AD2/C0_AD2：ADC conversion rate selection

C1	C0	ADC Conversion Time	SADC Line noise rejection
0	0	350ms	50/60Hz
0	1	175ms	50/60Hz
1	0	87.5ms	60Hz

AC_1/AC_2：AC mode control enable bit

Q2/Q1/Q0：Range control bit for V/A/R/C modes

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B2/B1/B0：Buzzer frequency selection

B2	B1	B0	Buzzer frequency
0	0	0	1.00kHz
0	0	1	2.67kHz
0	1	0	2.00kHz
0	1	1	3.33kHz
1	0	0	1.33kHz
1	0	1	3.08kHz
1	1	0	2.22kHz
1	1	1	4.00kHz

VAHZ_1/VAHZ_2：Frequency measurement for AC mode enabled control

FQ2_1/FQ1_1/FQ0_1/ FQ2_2/FQ1_2/FQ0_2：Range control bit for FREQ mode

PCAL_1/PCAL_2：Peak voltage detection offset calibration control bit

PEAK_1/PEAK_2：Peak hold measurement mode control bit

INA：Inrush indicator circuit ON/OFF control bit

FCOND：Conductance mode enabled control at 60MΩ range

AD2OFF：ADC2 disabled control

SUDP2_1/SUDP1_1/SUDP0_1：User-defined ADC1 input channel selection

SUDP2_2/SUDP1_2/SUDP0_2：User-defined ADC2 input channel selection

TMP24X_1/TMP24X_2：Full scale divided by 24 for UDP mode control bit

LPF1_1/LPF0_1/LPF1_2/LPF0_2：3dB BW for low-pass-filter selection

VHZ1K_1/VHZ1K_2：RC filter control bit for VAHz measurement

SWAP：ADC2 input is switched from ACVL2 & ACVH2 to ACVL1 & ACVH1

SHBP：Auxiliary low-resistance detection control bit for Continuity and Diode modes

DIOVSS：Diode measurement mode open-source voltage selection

INTSEL：Dynamically change the integration time to stabilize DC in AC+DC mode

UDPX10_2：Full scale change from 600.0mV to 60.00mV for UDP mode control bit

DR1/DR2/DR3/DR4：Open drain output

ZERODET：Period signal output control bit for VA dual mode

HRC：High RC range control bit for Resistance or capacitor measurement

T1300_1/T1300_2：Change the upper temperature limit from 600.0 to 1300

SGND2TOEXT：Switch one of ADC2 input from SGND2 pin to EXT pin

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The read command includes one ID byte with 16 data bytes. When DATANEW is ready[3], MPU could send the read data command to get the result of both ADCs conversion

[3] DATANEW will be active when one ADC conversion finished. DATANEW for frequency or capacitance mode will be active when D0 or D3 data ready.

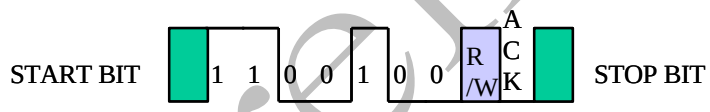
(D0/D1/D2/D3/D4)[4] or status flag from ES228. If the conversion rate of both ADCs is different, the status flag DRDY_D0/DRDY_D1 should be checked. If DRDY_D0=1, it means the D0 data is valid. If DRDY_D1=1, it means the D1 data is valid.

The next table shows the content of read command.

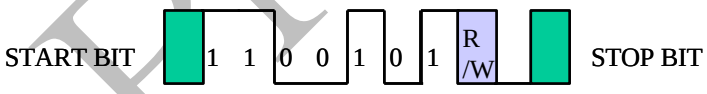
Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID	1	1	0	0	1	0	**BUZ**	**R/W=1**
R1	HV_AD1	HV_AD2	ALARM	DRDY_D0	DRDY_D1	RPH	VID1	VID2
R2	SIGN_1	SIGN_2	BTS0	BTS1	PMAX	PMIN	X	X
R3	DISC	LDUTY	STA1_1	STA1_2	FIN_1	STA1_2	STA0_2	FIN_2
R4	LF1	LF2	X	X	D0:0	D0:1	D0:2	D0:3
R5	D0:4	D0:5	D0:6	D0:7	D0:8	D0:9	D0:10	D0:11
R6	D0:12	D0:13	D1:0	D1:1	D1:2	D1:3	D1:4	D1:5
R7	D1:6	D1:7	D1:8	D1:9	D1:10	D1:11	D1:12	D1:13
R8	D1:14	D1:15	D1:16	D1:17	D1:18	D2:0	D2:1	D2:2
R9	D2:3	D2:4	D2:5	D2:6	D2:7	D2:8	D2:9	D2:10
R10	D2:11	D2:12	D2:13	D2:14	D2:15	D2:16	D2:17	D2:18
R11	D2:19	D3:0	D3:1	D3:2	D3:3	D3:4	D3:5	D3:6
R12	D3:7	D3:8	D3:9	D3:10	D3:11	D3:12	D3:13	D3:14
R13	D3:15	D3:16	D3:17	D3:18	D3:19	D4:0	D4:1	D4:2
R14	D4:3	D4:4	D4:5	D4:6	D4:7	D4:8	D4:9	D4:10
R15	D4:11	D4:12	D4:13	D4:14	D4:15	D4:16	D4:17	D4:18
R16	D4:19	X	X	X	X	X	X	X

Buzzer frequency selection: **B2/B1/B0**

Set B2-B0 properly to get the target frequency. Use **BUZ** control bit to enable/disable the *BUZOUT* (pin67) driver output. If MPU control BUZ only, it is available to set ID byte with ending of stop bit.



Buzzer OFF



Buzzer ON

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[4] D0/D1/D2/D3/D4 all are binary code format. D0 is ADC1 output and D1 is ADC2 output. The maximum data is 6300 counts for both ADCs.

Status flags for measurement mode: ● = function available

Measurement mode	HV_n	ALARM	LDUTY	STA0_n	STA1_n	FIN_n	PMAX	PMIN
V mode				●	●	●	●	●
A mode	●			●	●	●	●	●
VA dual mode	●			●	●	●	●	●
Res. mode	●							
Cont. mode	●	●						
Cap. mode	●	●						
Diode mode	●	●						
LED mode	●							
Hz+% mode	●	●	●	●	●	●		
UDP mode	●			●	●	●	●	●
Measurement mode	LF_n	SIGN_n	BTSn	DISC	RPH			
V mode	●	●	●					
A mode	●	●	●					
VA dual mode	●	●	●					
Res. mode			●		●			
Cont. mode			●					
Cap. mode			●	●				
Diode mode		●	●					
LED mode		●	●					
Hz+% mode	●		●					
UDP mode	●	●	●					

Description of status flags:

SIGN_1/SIGN_2: the sign bit of D0/D1, respectively.

HV_1/HV_2: When abnormal voltage applied to ADC1/ADC2, the flag will be set.

ALARM: Status flag will be set when short detection in Cont./Diode mode or larger capacitance detection or higher frequency indication in Hz mode

DISC: Status flag for capacitor discharging mode

BTS0/BTS1: Multi-level battery voltage indication

LF_1/LF_2: Lower frequency indication for Hz mode of ADC1/ADC2

LDUTY: Low duty indication for Hz + duty mode

STA0_1/STA1_1/STA0_2/STA1_2: divider indication for Hz mode of ADC1/ADC2.

FIN_1/FIN_2: Measurement cycle finished for Hz mode of ADC1/ADC2

PMAX: Indicate the ADC data (D0 or D1) is the output of peak maximum voltage

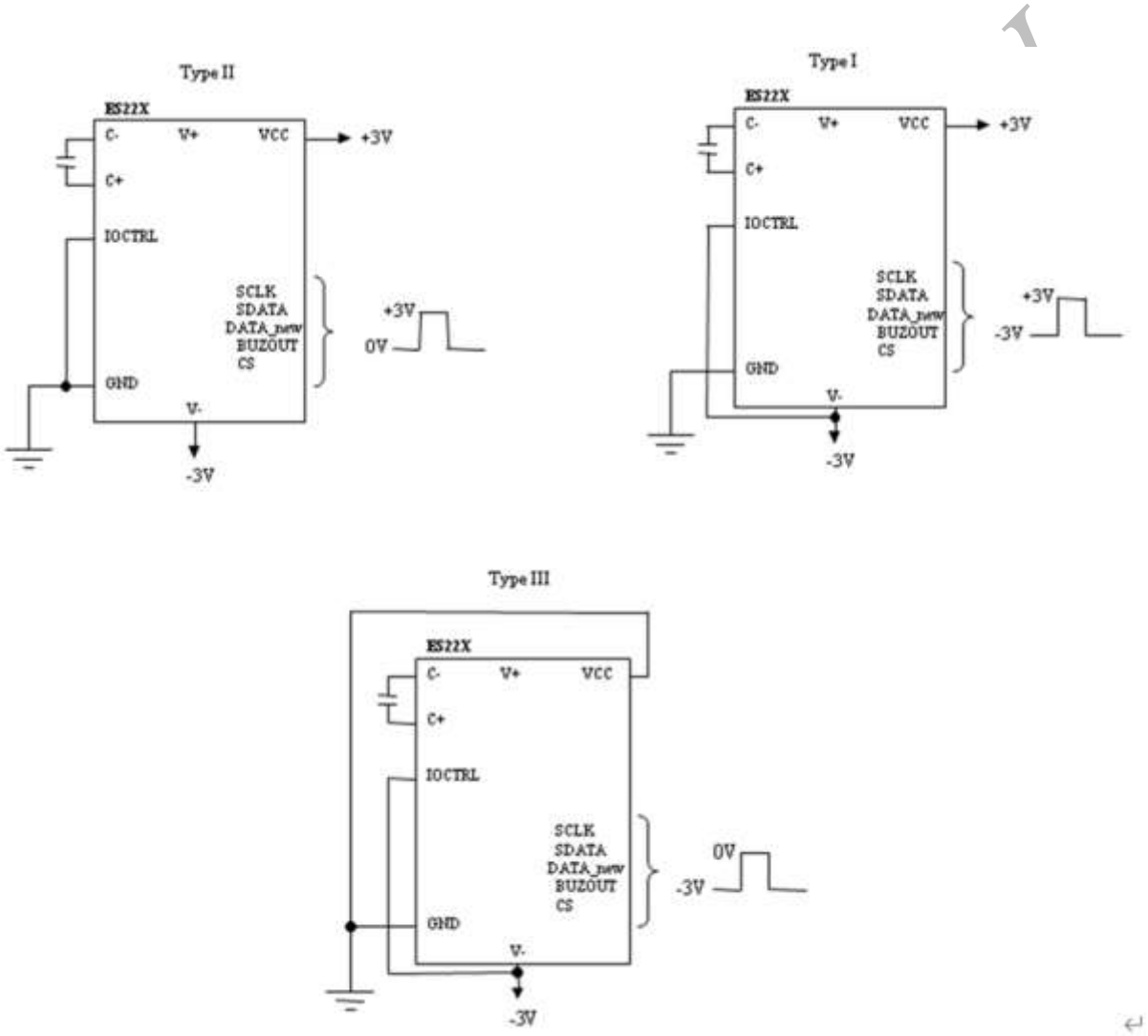
PMIN: Indicate the ADC data (D0 or D1) is the output of peak minimum voltage

RPH: ADC output indication bit for conductance mode

Preliminary

Power & I/O level selection

The ES228 provide a flexible I/O level setting for different MPU system configuration. The VCC should be connected to the same potential of external Vcc of MCU. The VCC is allowed to be set between DGND ~ V+. The IOCTRL pin selects the Vss level of MCU. If IOCTRL is set to DGND, the Vss level of MCU is the same as DGND. If IOCTRL is set to V-, the Vss level of MCU is the same as V-.



Operating Modes

DC&AC Voltage Measurement

MPU send write command to select the DC&AC voltage measurement function. The Hz mode measurement is available to be enabled by setting **VAHZ_2**=1 simultaneously. The measured signal is applied to *VR1* terminal (pin16) through 10MΩ.

See the next table of function command:

F3	F2	F1	F0	Measurement mode	Read data bytes
0	0	0	0	DCV&ACV mode	D0(0:13), D1(0:13), D3(0:19), D4(0:19)

Note: SIGN_1 & SIGN_2 are the sign bit of D0/D1, respectively.

Range control for voltage mode (DCV&ACV)

Q2	Q1	Q0	Full Scale Range	Divider Ratio	Resister Connection
0	0	0	6.000V	1/10	VR2 (1.111MΩ)
0	0	1	60.00V	1/100	VR3 (101kΩ)
0	1	0	600.0V	1/1000	VR4 (10.01kΩ)
0	1	1	1000V	1/10000	VR5 (1kΩ)
1	0	0	600.0mV	1	VR1 (10MΩ)

Frequency range control for ACV mode (set **VAHZ_2**=1)

FQ2_2	FQ1_2	FQ0_2	Full Scale Range
0	0	0	60.00Hz
0	0	1	600.0Hz
0	1	0	6.000kHz
0	1	1	60.00kHz

Note: See Frequency/duty cycle mode measurement.

Preliminary

DC&AC Current measurement

MPU send write command to select the DC&AC current measurement function. The Hz mode measurement is available to be enabled by setting **VAHZ_2**=1 simultaneously.

See the next table of function command:

F3	F2	F1	F0	Measurement mode	Read data bytes
0	0	0	1	DCA&ACA mode	D0(0:13), D1(0:13), D3(0:19), D4(0:19)

Note: SIGN_1 & SIGN_2 are the sign bit of D0/D1, respectively.

The external current sensed signal is applied to *UDP* terminals (pin19-24,27,28). The input channel is selected by write command as following: (Use multiple terminals to implement auto range scheme)

SUDP2_n[5]	SUDP1_n[5]	SUDP0_n[5]	Full Scale Range[6]	Input terminals
0	0	0	600.0mV	UDPIN1
0	0	1	600.0mV	UDPIN2
0	1	0	600.0mV	UDPIN3
0	1	1	600.0mV	UDPIN4
1	0	0	600.0mV	UDPIN5
1	0	1	600.0mV	UDPIN6
1	1	0	600.0mV	UDPIN7
1	1	1	600.0mV	UDPIN8

Frequency range control for ACA mode (set **VAHZ_2**=1)

FQ2_2	FQ1_2	FQ0_2	Full Scale Range
0	0	0	60.00Hz
0	0	1	600.0Hz
0	1	0	6.000kHz
0	1	1	60.00kHz

Note: See Frequency/duty cycle mode measurement**..**

Preliminary

[5] n should be 1 & 2.

[6] Full scale range could be changed from 600.0mV to 60.00mV when UDPX10_2=1.

Low pass filter (LPF) mode for ACA/ACV mode

A 2nd order low pass filter with is built in ES228. The 3dB bandwidth of the low pass filter could be selectable by MPU. The LPF mode is enabled when the LPF control bit is set to be active. The low pass filter control bit could be set individually for ADC1 or ADC2

.

LPF1_n[7]	LPF0_n[7]	Low pass filter effect
0	0	Disable
0	1	3dB = 1kHz
1	0	3dB = 10kHz
1	1	3dB > 100kHz

Preliminary

[7] n should be 1 & 2 simultaneously.

VA dual mode measurement

MPU send write command to select the voltage/current dual measurement function. The voltage & current sensed signal could be applied into meter simultaneously. The Hz mode measurement is available to be enabled by setting **VAHZ_1**=1 / **VAHZ_2**=1. The voltage measured signal is applied to *VR1* terminal (pin16) through 10MΩ in V/A dual mode.

F3	F2	F1	F0	AC_1	AC_2	Measurement mode	Read data bytes[8]
0	0	1	1	0	0	DCV&DCA mode	D0(0:13), D1(0:13), D2(0:19), D3(0:19), D4(0:19)
0	0	1	1	1	1	ACV&ACA mode	D0(0:13), D1(0:13), D2(0:19), D3(0:19), D4(0:19)

Range control for voltage mode (DCV or ACV)

Q2	Q1	Q0	Full Scale Range	Divider Ratio	Resister Connection
0	0	0	6.000V	1/10	VR2 (1.111MΩ)
0	0	1	60.00V	1/100	VR3 (101kΩ)
0	1	0	600.0V	1/1000	VR4 (10.01kΩ)
0	1	1	1000V	1/10000	VR5 (1kΩ)
1	0	0	600.0mV	1	VR1 (10MΩ)

The external current sensed signal is applied to *UDP* terminals (pin19-24,27,28). The input channel is selected by write command as following: (It is possible to use multiple terminals to implement auto range scheme)

SUDP2_2	SUDP1_2	SUDP0_2	Full Scale Range[9]	Input terminals
0	0	0	600.0mV	UDPIN1
0	0	1	600.0mV	UDPIN2
0	1	0	600.0mV	UDPIN3
0	1	1	600.0mV	UDPIN4
1	0	0	600.0mV	UDPIN5
1	0	1	600.0mV	UDPIN6
1	1	0	600.0mV	UDPIN7
1	1	1	600.0mV	UDPIN8

Frequency range control for ACV or ACA mode (set **VAHZ_1**=1 / **VAHZ_2**=1)

FQ2_n[10]	FQ1_n[10]	FQ0_n[10]	Full Scale Range
0	0	0	60.00Hz
0	0	1	600.0Hz
0	1	0	6.000kHz
0	1	1	60.00kHz

Note1: See Frequency/duty cycle mode measurement.

Note2: n should be 1 or 2 depends on whether VAHZ_1 or VAHZ_2 is set or not.

[8] D0/D1/D2/D3/D4 all are binary format. SIGN_1 & SIGN_2 are the sign bit of D0/D1, respectively.

[9] Full scale range could be changed by UDPX10_2.

[10] n should be 1 & 2 simultaneously.

Preliminary

Resistance/Conductance Measurement

MPU send write command to select the resistance measurement function.

F3	F2	F1	F0	Measurement mode	Read data bytes[11]
0	1	1	1	Resistance mode	D0(0:13), D1(0:13)[12]

Range control for resistance mode

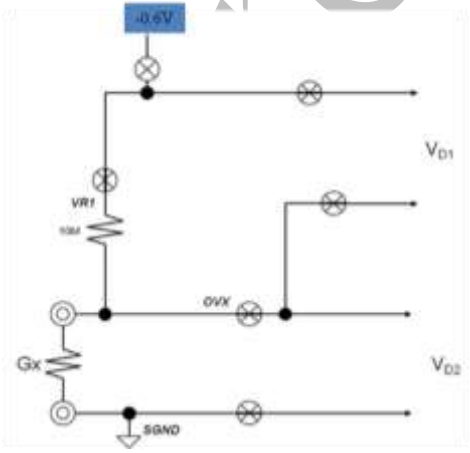
Q2	Q1	Q0	HRC	Full Scale Range	Relative Resistor	Equivalent value
0	0	0	0	600.0Ω	OR1	100Ω
0	0	1	0	6.000KΩ	VR5	1KΩ
0	1	0	0	60.00KΩ	VR4 || VR1	10KΩ
0	1	1	0	600.0KΩ	VR3 || VR1	100KΩ
1	0	0	0	6.000MΩ	VR2 || VR1	1MΩ
1	0	1	0	60.00MΩ	VR1	10MΩ
1	0	1	1	300.0MΩ	VR1	10MΩ
1	1	1	0	60.00Ω	OR1	100Ω

Set FCOND=1 when range control is 60MΩ range, the conductance mode is available. The status RPH bit is used for converted data indication of reference voltage or input voltage.

Q2	Q1	Q0	FCOND	Full Scale Range	Relative Resistor	Equivalent value
1	0	1	1	600nS	VR1	10MΩ

The maximum displayed count is 600 and the resolution should be 1nS. The MCU should check the status bit RPH and D0 simultaneously. When RPH=1 the D0 data should be V_{D1}. If RPH=0, then the D0 data should be V_{D2}. The DUT conductance value could be calculated by simple formula.

$$Gx = V_{D1}/V_{D2} * 1000$$



[11] D0/D1 both are binary format. SIGN_2 is the sign bit of D1. Resistance value is D0

[12] If AD2OFF =0, D1 data is the ADC result of UDP terminals.

preliminary

Capacitance Measurement

MPU send write command to select the capacitance measurement function.

Function code of capacitance measurement

F3	F2	F1	F0	Measurement mode	Read data bytes[13]
1	0	0	1	Capacitance mode	D0(0:13), D1(0:13)[14]

Range control for capacitance measurement

Q2	Q1	Q0	HRC	Full Scale Range	Relative Resistor	Measurement Period
0	0	0	0	6.000nF	OVX pin VR	0.33 sec
0	0	1	0	60.00nF	OVX pin VR	0.33 sec
0	1	0	0	600.0nF	-	1.15 sec max.
0	1	1	0	6.000uF	R9K / R1K	0.2 sec max.
1	0	0	0	60.00uF	R9K / R1K	0.5 sec max.
1	0	1	0	600.0uF	R9K / R1K	1.25 sec max.
1	1	0	0	6.000mF	R9K / R1K	2.5 sec max.
1	1	1	0	60.00mF	R9K / R1K	12.5 sec max.
1	1	1	1	300.0mF	R9K / R1K	31.25 sec max.

When the ALARM bit is set, it means that the value exceeds the current measurement range. This can quickly increase the measurement range.

Quickly change measurement range.

ALARM = 1	Current Range	Next Range
	< 6.000uF	6.000uF
	6.000uF ~ 600.0uF	6mF

DISC status bit is used for detection of DUT capacitor voltage. If DISC=1, the internal capacitor discharging mode is active and the capacitance measurement is inhibited. It is recommended to discharge the DUT capacitor externally.

[13] D0/D1 both are binary format. SIGN_2 is the sign bit of D1. Resistance value is D0

[14] If AD2OFF=0, D1 data is the ADC result of UDP terminals.

Preliminary

Continuity Check

MPU send write command to select the continuity measurement function.

Function code of Continuity measurement

F3	F2	F1	F0	Measurement mode	Read data bytes[15]
1	0	0	0	Continuity mode	D0(0:13), D1(0:13)[16]

Continuity mode shares the same configuration with 600.0Ω resistance measurement circuit and support the low-resistance detection. If the *STBEEP* output (pin64) is low, it means the low-resistance status is detected (It means the *OVX* terminal voltage less than -7mV). It could be faster than the ADC1 result, so MPU could monitor the *STBEEP* output and ADC1 (D0) data output make the high speed detection for short circuit detection. Set **SHBP**=1 to enable the built-in buzzer driving automatically when *STBEEP* is active.

Diode/LED mode Measurement

MPU send write command to select the diode or LED measurement function.

Diode/LED function code

F3	F2	F1	F0	Measurement mode	Read data bytes[17]
1	0	1	0	Diode mode	D0(0:13), D1(0:13)[16]
1	0	1	1	LED mode	D0(0:13), D1(0:13)[16]

Diode measurement mode shares the same configuration with 6.000V voltage measurement circuit and support the low-resistance detection. If the *STBEEP* output (pin64) is low, it means the low-resistance status is detected (It means the *OVX* terminal voltage less than 9mV). It could be faster than the ADC1 result, so MPU could monitor the *STBEEP* output and ADC1 (D0) data output make the high-speed detection for short circuit detection. Set **SHBP**=1 to enable the built-in buzzer driving automatically when *STBEEP* is active. The default source voltage at diode mode is the same as V+ potential. Set **DIOVSS**=1 when diode measurement to change source voltage from V+ to V- potential.

Because some LED device will need higher voltage source to turn on, so MPU could select LED mode to change the source voltage to external source. The external voltage source (positive or negative) applied from rotary switch.

Preliminary

[15] D0/D1 both are binary format. SIGN_2 is the sign bit of D1. Resistance value is D0.

[16] If AD2OFF=0, D1 data is the ADC result of UDP terminals.

[17] D0/D1 both are binary format. SIGN_1 & SIGN_2 are the sign bit of D0/D1, respectively. Diode voltage value is D0.

Frequency/duty cycle mode measurement

MPU send write command to select the frequency mode measurement.

Function code of frequency measurement

F3	F2	F1	F0	Measurement mode	Read data bytes
1	1	0	0	Hz/ Duty mode	D0(0:13), D1(0:13)[18], D2(0:19), D3(0:19)

Range control for frequency measurement

FQ2_1	FQ1_1	FQ0_1	Full Scale	Conversion period
0	0	0	60.00Hz	350ms (fixed)
0	0	1	600.0Hz	350ms (fixed)
0	1	0	6.000KHz	350ms (fixed)
0	1	1	60.00KHz	350ms (fixed)
1	0	0	600.0KHz	350ms (fixed)
1	0	1	6.000MHz	350ms (fixed)
1	1	0	60.00MHz	350ms (fixed)

Available minimum frequency input F_{MIN} = 1.00Hz

Calculation for Frequecy.

Flag	STA0[19]=1	STA0[19]=0	
Range		STA1[19]=1	STA1[19]=0
60.00Hz	FREQ=100000000/D3[20]	FREQ=400000000/D3[20]	FREQ=1600000000/D3[20]
600.0Hz	FREQ=10000000/D3[20]	FREQ=80000000/D3[20]	FREQ=640000000/D3[20]
6.000KHz	FREQ=1000000/D3[20]	FREQ=4000000/D3[20]	FREQ=256000000/D3[20]
60.00KHz	FREQ = ADC counter (D0)[21]		
600.0KHz			
6.000MHz			
60.00MHz			

The duty cycle measurement range is 5.0%~95.0% , 0.1% resolution is recommended.

Calculation for duty

Status Flag	LDUTY=1	LDUTY=0
Duty cycle (<10kHz)	10000-D2*10000/D3	D2*10000/D3

The status flag FIN indicates the frequency input signal available (> F_{MIN}) or not. If the

[18] If AD2OFF=0, D1 data is the ADC result of UDP terminals.

[19] If Hz+duty mode is selected or VAHZ_1 is set to active, assign STA0= STA0_1 & STA1=STA1_1 & FIN=FIN_1. If VAHZ_2 is set to active, assign STA0= STA0_2 & STA1=STA1_2 & FIN=FIN_2.

[20] If VAHZ_1 is active, D3 should be replaced by D2.

[21] If VAHZ_1 is active, ADC counter will be D2. If VAHZ_2 is active, ADC counter will be D3.

Preliminary

computed result less than F_{MIN}, the frequency/duty cycle readings should be set to zero.

The status flags ALARM & LF are used for fast judgment of proper range. If frequency input is larger than 8 kHz, ALARM will be active. If frequency input is floating or frequency detected too low, LF will be active.

Auto range consideration for MPU by using Status Flag of frequency mode

<table>
<tr><th>Flag
Range</th><th>FIN=0</th><th>FIN=0 or 1</th><th colspan="2">FIN=1</th></tr>
<tr><th></th><th>LF=0</th><th>LF=1[22]</th><th>ALARM=LF=0</th><th>ALARM=1[23]</th></tr>
<tr><td>60.00Hz
600.0Hz
6.000KHz</td><td rowspan="2">Data and Range is not necessary to be updated</td><td>Hz/Duty=0</td><td rowspan="2">Change range depends on data computed</td><td>Set range to 60.00kHz range</td></tr>
<tr><td>60.00KHz
600.0KHz
6.000MHz
60.00MHz</td><td>Set range to 60.00Hz range</td><td>Change range depends on data computed</td></tr>
</table>

Duty cycle mode range (Input sensitivity > 2Vpp @ duty cycle = 5.0% & 95.0%)

Freq. range	Duty range*
60.00Hz 600.0Hz	5.0% - 95.0%
6.000KHz	10.0 % - 90.0%

Preliminary

22 LF=1 @ 60Hz range implies the frequency is not available to be measured. The Hz/Duty readings should be set to zero.

23 When VAHZ mode is selected, the ALARM status should be ignored. Change range depends on data calculation result.

UDP dual mode

MPU send write command to select the UDP mode measurement function. The signal full scale is 600mV for DC/AC mode.

The UDPX10_2 control bits set the full scale from 600.0mV to 60.00mV.

The AC_1/AC_2 control bits set the AC mode.

The VAHZ_1/VAHZ_2 control bits set the Hz mode.

Function code for UDP mode

F3	F2	F1	F0	Measurement mode	Read data bytes
1	1	0	1	UDP dual mode	D0(0:13), D1(0:13), D2(0:19), D3(0:19)

The measured signal is applied to *UDP* terminals (pin19-24,27,28). The input channel is selected by write command as following:

Input channel selection code for UDP

SUDP2_n[24]	SUDP1_n[24]	SUDP0_n[24]	Input terminals
0	0	0	UDPIN1
0	0	1	UDPIN2
0	1	0	UDPIN3
0	1	1	UDPIN4
1	0	0	UDPIN5
1	0	1	UDPIN6
1	1	0	UDPIN7
1	1	1	UDPIN8

Frequency range control for AC mode (set **VAHZ_1**=1 or **VAHZ_2**=1)

FQ2	FQ1	FQ0	Full Scale Range
0	0	0	60.00Hz
0	0	1	600.0Hz
0	1	0	6.000kHz
0	1	1	60.00kHz

Preliminary

24 When n=1, the input terminal will be set to ADC1 (D0). When n=2, the input terminal will be set to ADC2 (D1).

Dynamically Adjusting Integration Time (only support for DCV&ACV or DCA&ACA)

The ADC integration time of ES228 can be selected from 200ms, 100ms and 50ms.
When ES228 measures a signal with AC, it will convert it into a DC signal. However, converted DC always contains ripples at the frequency of the AC signal. If the period time of the ripple is a low frequency signal and the integration time is not divisible by the period time of the ripple, the ADC reading will be unstable.
Setting INTSEL can dynamically change the integration time according to the signal being measured.

Related control bits

Control bit	State	Description
INTSEL	1	Integration time is dynamic.
	0	Integration time is fixed.

Formula 1. Reading when INTSEL = 1

$$Reading = 200000 \times \frac{Dn^{25}}{D4}$$

If the frequency is lower than 30Hz the circuit will not work properly. It will have no effect.

Preliminary

[25] n is 0 or 1,

Inrush Indicator Circuit

ES228 provides an inrush indicator circuit. Only supported in ACA/UDP(AC) mode. Set the control bit INA=1 of write command to enable the inrush indicator circuit.

In inrush measurement, the inrush indicator circuit must be used with an external fast ADC.

The inrush measurement steps:

1. Set INA bit to enable the inrush indicator circuit.
2. Waiting for an inrush signal. When an inrush signal comes, INRUSHOUT pin is set to a high level to trigger the external ADC.
3. Use an external fast ADC to sample the inrush signal from ADO pin.
4. Clear INA bit twice to disable the inrush indicator circuit, or set INA bit again to restart inrush indicator circuit.

Related control bits

Control bit	State	Description
INA & BYPASS	1	Enable inrush indicator circuit
	0	Disable inrush indicator circuit (must be written twice)

Related pins

Pin	Description
ADO	Signal output.
INRUSHOUT	Set to high when inrush signal is detected.

Preliminary

Zero crossing detector

ES228 built in a zero-crossing detector circuit. It can use to detect the frequency of AC signal. Set AC_1=1, AC_2=1, ZERODET=1 and LPF=1 to enable the zero-crossing detector circuit. When the signal crosses zero, the DR3 and DR4 pins will output a high or a low to indicate the rising or falling edge. However, the comparison level for zero-crossing detection is fixed. Since signals of different amplitudes have different delay times, they cannot be used for phase judgment.

Related control bits

Control bit	State	Description
ZERODET	1	Enable Zero-crossing detector circuit
	0	Disable zero-crossing detector circuit
LPF	1 or 2	Enable Low pass filter with BW=1kHz or 10kHz.

Preliminary

Peak-hold measurement mode

Introduction

ES228 provides a peak hold function to capture the real peak value for voltage or current measurement mode. In a case of a 1V sine wave input voltage, the peak hold function gets a maximum peak value of 1.414V and minimum peak value of –1.414V ideally. Set the control bit **PEAK_1=1 or PEAK_2 =1** to force the ES228 entering PEAK hold measurement mode for ADC1 (D0) or ADC2 (D1). The PEAK_1 & PEAK_2 are not allowed to set simultaneously. Peak Hold function is divided into three parts of peak maximum, peak minimum & current RMS conversion. The ADC performs peak maximum / current value and peak minimum / current value conversion sequentially, not at the same time. The status flag PMAX or PMIN shows that type of the peak value. If PMAX=1(PMIN=1), the ADC output (D0 or D1) is the conversion data on *PMAX (PMIN)* terminals (pin 58/59). The MPU should make the comparison procedure to get the maximum value of *PMAX* data and minimum value of *PMIN* data. If PMAX=0 & PMIN=0, that means ADC is the current RMS value conversion result.

Peak calibration mode

At PEAK-Hold measurement mode, the offset voltage of internal operation amplifier(OPA) will cause an error. To obtain a more accurate value, the offset error must be canceled. ES228 provides the peak calibration feature to remove the influence on accuracy by internal offset voltage. Set the control bit **PCAL**=1 & **PEAK**=1 simultaneously enter peak calibration mode. In peak calibration mode is active, the ADC of ES228 will output the OPA offset value of peak maximum and minimum conversion in turn. The offset values should be memorized respectively and deducted from the data of *PMAX/PMIN* at the normal peak measurement mode. (PMAX = VPMAX_current_value – VPMAX_offfset & PMIN = VPMIN_current_value – VPMIN_offset)

Set PEAK=1 or PCAL=1		
Status indication	**PMAX=1, PMIN=0**	**PMAX=0, PMIN=1**
ADC data	$V_{PMAX.C}$	$V_{PMIN.C}$

$V_{PMAX.C}$ and $V_{PMIN.C}$ are not the real-time value of peak-hold voltage. They are the voltage stored on terminal capacitor (pin58-59). Because the capacitor will be self-discharging, so MCU need to compare the $V_{PMAX.C}$ & $V_{PMIN.C}$ respectively and memorize the maximum and minimum peak values in turn.

Preliminary

Logic Output

ES228 has four open drain outputs, DR1, DR2, DR3 and DR4. MPU can set or clear DR1, DR2, DR3 and DR4 in the write command to output logic high or low. The DR3 and DR4 pin are share with the zero-crossing detector function.

Sleep

Set *CS* pin (pin 62) to logic low to make the ES228 entering the sleep mode. The current consumption will be less than 25uA typically. Set *CS* pin to logic high or kept floating, the ES228 will return to normal operation.

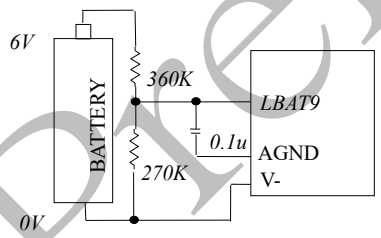
Multi-level battery voltage indication

The ES228 is built-in a comparator for batter voltage indication. The voltage is applied to *LBAT9* pin (pin 80) vs. *V-* terminal. MPU could check the status bit BTS1/BTS0 and monitor the *LBAT9* voltage status.

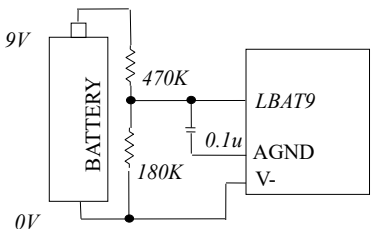
Battery voltage	BTS1	BST0
$V_{LBT} > V_{t1}$	1	1
$V_{t2} < V_{LBT} < V_{t1}$	1	0
$V_{t3} < V_{LBT} < V_{t2}$	0	1
$V_{LBT} < V_{t3}$	0	0

Low battery configuration for 9V/1.5V*4/1.5V*3 battery

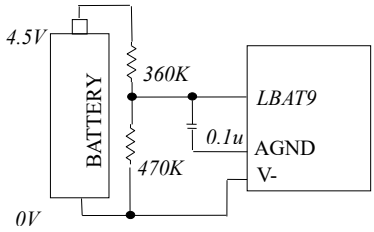
Low battery test circuit (a)



Low battery test circuit (b)

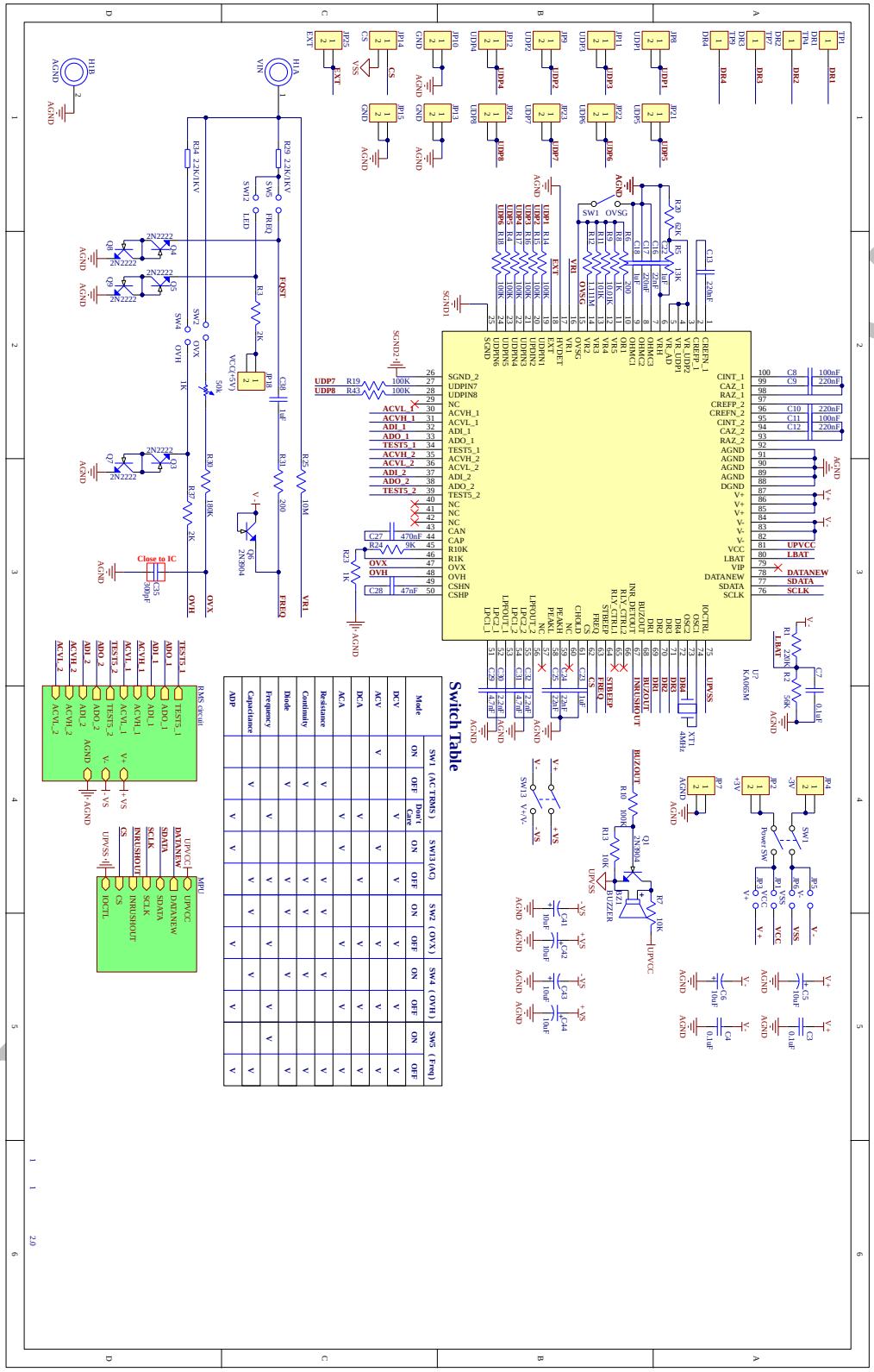


Low battery test circuit (c)



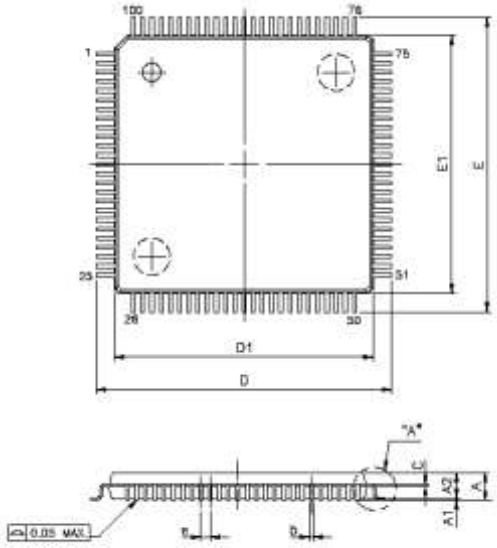
Preliminary

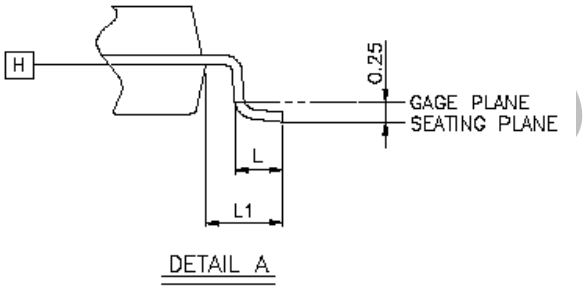
Application Circuit



The RMS circuit can refer to ES26 or ES5 or ES736 application circuit.

Package Information
100L LQFP Outline drawing





DETAIL A

Dimension parameters

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

NOTES:
1.JEDEC OUTLINE:
MS-026 BHB.
MS-026 BHB-HD(THERMALLY ENHANCED VARIATIONS ONLY).
2.DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS E1 AND D1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS E AND E DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H]
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .

Revision

V2.4：Modified the values of LPC1 (1nF->4.7nF) and LPC2 (470pF->2.2nF) in the application circuit……2025-03-19

Preliminary