承永資訊科技
CYRUSTEK CO.

ES222(9999counts dual)

DMM Analog front end/Inrush

Features

- 9999 counts dual ADC core (2.8-22 cnvs/s.)
- Input signal full scale: 100mV
- 128L LQFP package
- 3V DC regulated power supply
- Support digital multi-meter function

  *Voltage measurement (AC/DC)

  *Current measurement (AC/DC)

  *Support AC+DC RMS mode

  *Dual mode for AC/DC voltage or current

  *Resistance measurement (0.00Ω – 99.99MΩ)

  *Conductance measurement (199.9 nS)

  *Capacitance measurement (0.000nF – 99.9mF)
  (Taiwan patent no.: 323347, 453443)

  (China patent no.: 200710106702.8)

  *Diode or continuity mode measurement

  *Frequency counter with duty cycle display:

  1.00Hz – 40.00MHz

  5.0% – 95.0%
- User-defined ADP mode
- Support Inrush mode or Peak-hold mode
- Hazard voltage indication for R/C/D/F modes
- 3dB BW selectable for low pass filter (dual) at AC mode
  (**Taiwan patent no.: 362409**)
  (**China patent no.: 200920156001.X**)
- Band-gap reference voltage output
- 3-wire serial bus for MPU I/O port
- MPU I/O power level selectable by external pins
- On-chip buzzer driver and frequency selectable by MPU command
- Multi-level battery voltage detection
- Support sleep mode by external chip select pin

Application

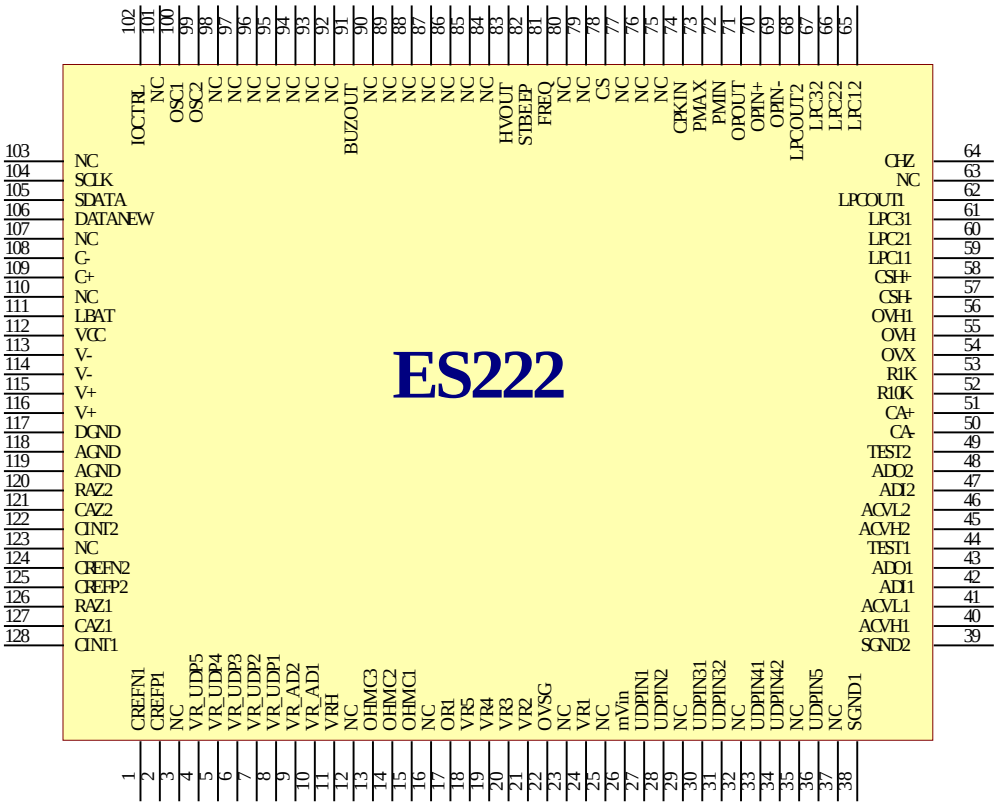
Clamp-on meter

Digital multi-meter

Description

ES222 is an analog frond end chip of DMM built-in dual 9999 counts dual-slope ADCs. The dual ADC cores are fully operated individually. . ES222 provides voltage & current (AC/DC) measurement, resistance measurement, capacitance measurement, diode/continuity measurement, frequency measurement and duty cycle measurement ES222 also supports multi-level battery detection, low-pass-filter feature for AC mode and dual mode measurement for ACV+ACA, ACV+DCV, DCV+DCA, ACA+DCA, V+F & A+F. A 3-wire serial bus for MPU I/O port will be used easily for firmware design. Flexible function design is supported for different kinds of DMM or Clamp-on meter application.

Pin Assignment



Pin Description

Pin No	Symbol	Type	Description
1	CREFN1	O	Negative connection for reference capacitor of ADC1.
2	CREFP1	O	Positive connection for reference capacitor of ADC1.
3	NC	-	No connection.
4	VR_UDP5	I	Reference input voltage in UDP5 mode. Typically –200mV
5	VR_UDP4	I	Reference input voltage in UDP4 mode. Typically –200mV
6	VR_UDP3	I	Reference input voltage in UDP3 mode. Typically –200mV
7	VR_UDP2	I	Reference input voltage in UDP2 mode. Typically –200mV
8	VR_UDP1	I	Reference input voltage in UDP1 mode. Typically –200mV
9	VR_AD2	I	Reference input voltage in ADC2 mode. Typically –200mV
10	VR_AD1	I	Reference input voltage in ADC1 mode. Typically –200mV
11	VRH	O	Output of band-gap voltage reference. Typically –1.23V
12	NC	-	No connection.
13-15	OHMC1-3	O	Filter capacitor connection1-3 for resistance mode.
16	NC	-	No connection.
17	OR1	O	Reference resistor connection for 100.00Ω range
18	VR5	O	Voltage measurement ÷9999 attenuator(1000.0V)
19	VR4	O	Voltage measurement ÷1000 attenuator(100.00V)
20	VR3	O	Voltage measurement ÷100 attenuator(10.000V)
21	VR2	O	Voltage measurement ÷10 attenuator(1.0000V)
22	OVSG	O	Sense low voltage for resistance/voltage measurement
23	NC	-	No connection.
24	VR1	I	Measurement Input. Connect to a precise 10MΩ resistor.
25	NC	-	No connection.
26	mVin	I	mV measurement input terminal.
27	UDPIN1	I	UDP1 mode input terminal.
28	UDPIN2	I	UDP2 mode input terminal.
29	NC	-	No connection
30	UDPIN31	I	UDP3 mode input terminal1.
31	UDPIN32	I	UDP3 mode input terminal2.
32	NC	-	No connection
33	UDPIN41	I	UDP4 mode input terminal1.
34	UDPIN42	I	UDP4 mode input terminal2.
35	NC	-	No connection
36	UDPIN5	I	UDP5 mode input terminal.
37	NC	-	No connection
38	SGND1	I/G	Signal ground for ADC1.
39	SGND2	I/G	Signal ground for ADC2.
40	ACVH1	I	DC signal high input in ADC1_AC mode. Connect to positive output of external AC to DC converter.
41	ACVL1	I	DC signal low input in ADC1_AC mode. Connect to positive output of external AC to DC converter.
42	ADI1	I	Negative input of internal AC to DC OP Amp for ADC1_AC mode.
43	ADO1	O	Output of internal AC to DC OP Amp for ADC1_AC mode.
44	TEST51	O	Buffer output of SGND1 for ADC1_AC mode
45	ACVH2	I	DC signal high input in ADC2_AC mode. Connect to positive output of external AC to DC converter.
46	ACVL2	I	DC signal low input in ADC2_AC mode. Connect to positive output of external AC to DC converter.
47	ADI2	I	Negative input of internal AC to DC OP Amp for ADC2_AC mode.
48	ADO2	O	Output of internal AC to DC OP Amp for ADC2_AC mode.
49	TEST52	O	Buffer output of SGND1 for ADC2_AC mode
50-51	CA-/CA+	O	Auto-zero capacitor connection for capacitor measurement
52	R10K	O	Connect to a precise 10KΩ resister for capacitor measurement.

53	R1K	O	Connect to a precise 1KΩ resister for capacitor measurement.
54	OVX	I	Sense input for resistance/capacitance measurement
55	OVH	O	Output connection for resistance measurement
56	OVH1	O	Output connection for resistance measurement (Optional)
57-58	CSH-/CSH+	O	Capacitor connection for inrush mode
59	LPC11	O	Capacitor C1 connection for internal low-pass filter of ADC1
60	LPC21	O	Capacitor C2 connection for internal low-pass filter of ADC1
61	LPC31	O	Capacitor C3 connection for internal low-pass filter of ADC1
62	LPCOUT1	O	Capacitor C1 connection for internal low-pass filter of ADC1
63	NC	-	No connection
64	CHZ	O	Internal filter for VA_Hz mode
65	LPC12	O	Capacitor C1 connection for internal low-pass filter of ADC2
66	LPC22	O	Capacitor C2 connection for internal low-pass filter of ADC2
67	LPC32	O	Capacitor C3 connection for internal low-pass filter of ADC2
68	LPCOUT2	O	Capacitor C1 connection for internal low-pass filter of ADC2
69-70	OPIN-/OPIN+	I	Individual OPAMP negative/positive input terminal.
71	OPOUT	O	Individual OPAMP output terminal.
72	PMIN	O	Minimum peak hold output
73	PMAX	O	Maximum peak hold output.
74	CPKIN	I	Bypass capacitor for peak mode
75-77	NC	-	No connection
78	CS	I	Chip selection input.
79-80	NC	-	No connection
81	FREQ	I	Frequency counter input, offset V-/2 internally by the chip.
82	STBEEP	O	Fast low-impedance sensed output for CONT./Diode mode
83	HVOUT	O	Improper voltage indication for ADC
84-90	NC	-	No connection
91	BUZOUT	O	Buzzer output driver
92-98	NC	-	No connection
99-100	OSC1/OSC2	-	4MHz crystal oscillator connection
101	NC	-	No connection
102	IOCTRL	I	MCU I/O logic low level setting
103	NC	-	No connection
104	SCLK	I	MCU serial clock input
105	SDATA	I/O	MCU serial data input
106	DATANEW	O	Data ready output.
107	NC	-	No connection
108-109	C-/C+	O	Capacitor connection for on-chip DC-DC converter.
110	NC	-	No connection
111	LBAT	I	Multi-level low battery configuration input. Simple external resistor divider is required.
112	VCC	P	MCU power connection
113-114	V-	P	Negative supply voltage.
115-116	V+	O/P	Output of on-chip DC-DC converter and positive supply voltage.
117	DGND	G	Digital ground.
118-119	AGND	G	Analog ground.
120	RAZ2	O	Buffer output pin in AZ and ZI phase for ADC2.
121	CAZ2	O	Auto-zero capacitor connection for ADC2.
122	CINT2	O	Integrator output for ADC2. Connect to integral capacitor.
123	NC	-	No connection
124	CREFN2	O	Negative connection for reference capacitor of ADC2.
125	CREFP2	O	Positive connection for reference capacitor of ADC2.
126	RAZ1	O	Buffer output pin in AZ and ZI phase for ADC1.
127	CAZ1	O	Auto-zero capacitor connection for ADC1.
128	CINT1	O	Integrator output for ADC1. Connect to integral capacitor.

Ab1solute Maximum Ratings

Characteristic	Rating
Supply Voltage (V- to AGND)	-4V
Analog Input Voltage & EXTSRC pin	V- -0.6 to V+ +0.6
V+	V+ ≥ (AGND/DGND+0.5V)
AGND/DGND	AGND/DGND ≥ (V- -0.5V)
Digital Input (IOCTRL=V-)	V- -0.6 to VCC+0.6
Power Dissipation. Flat Package	500mW
Operating Temperature	-20℃ to 70℃
Storage Temperature	-55℃ to 125℃

Electrical Characteristics

TA=25℃, V- = -3.0V

Parameter	Symbol	Test Condition	Min.	Typ.	Max	Units
Power supply	V-		-2.8	-3.0	-3.2	V
Operating supply current In DCV+DCA mode	I_{DD}	Normal operation	—	2.5	—	mA
	I_{SS}	In sleep mode	—	11	—	µA
ADC Voltage roll-over error		10MΩ input resistor	—	—	±0.02	%F.S[1]
ADC voltage nonlinearity	NLV1	Best case straight line	—	—	±0.02	%F.S[1]
Voltage full scale range of ADC		VA+-VA- = 200mV	—	100	120	mV
Input Leakage for VR1 input			-10	1	10	pA
Zero input reading		10MΩ input resistor	-000	000	+000	Count
Band-gap reference voltage	V_{RH}	100KΩ resistor between VRH and AGND	-1.30	-1.22	-1.14	V
Open circuit voltage for 100Ω range measurement			—	V-	—	V
Open circuit voltage for other Ω measurement			—	-1.04	—	V
Open circuit voltage for 199.9 nS conductance measurement			—	-0.6	—	V
Internal pull-high to 0V current		Between V- pin and CS	—	1.2	—	µA
AC frequency response at 6.000V range		±1%	—	40-400	—	HZ
		±5%	—	400-2000	—	
OP unity gain bandwidth	GB	C_L=10pF	—	200	—	kHz
OP slew rate at unity gain	SR	R_L=10MΩ	—	3.5	—	V/us
OP input offset voltage	V_{IO}		—	0.1	—	mV
OP input bias current	I_B		—	10	—	pA
OP input common mode voltage range	V_{ICR}		—	±2	—	V
3dB frequency for LPF[2] active	f_{3dB}	3dB=Full (ADP)	100	—	—	kHz
		3dB=10k (ADP)	—	10	—	kHz
		3dB=1k (ADP)	—	1	—	kHz

Multi-level low battery detector	V_{t1}	LBAT vs. V-	—	2.29	—	V
	V_{t2}		—	2.14	—	V
	V_{t3}		—	1.88	—	V
Peak-hold mode pulse width		ACIN =40 ~ 400Hz	—	1000	—	us
STBEEP comparator in Diode mode		OVX to SGND	—	+9	—	mV
STBEEP comparator in Cont. mode		OVX to SGND	—	-7	—	mV
Inrush triggered level		UDPn to SGND		+7		mV
Inrush measurement integration time			—	100	—	ms
Frequency input sensitivity (*FREQ*)	Fin	Square wave with Duty cycle 40-60%	500	—	—	mVp
Frequency input sensitivity (*FREQ*)	Fin	Sine wave	400	—	—	mVrms
Reference voltage temperature coefficient	TC_{RF}	100KΩ resister Between VRH -20℃<TA<70℃	—	75	—	ppm/℃
Capacitance measurement Accuracy		10nF – 100mF	-2.5	—	2.5	%F.S
			-30	—	30	counts

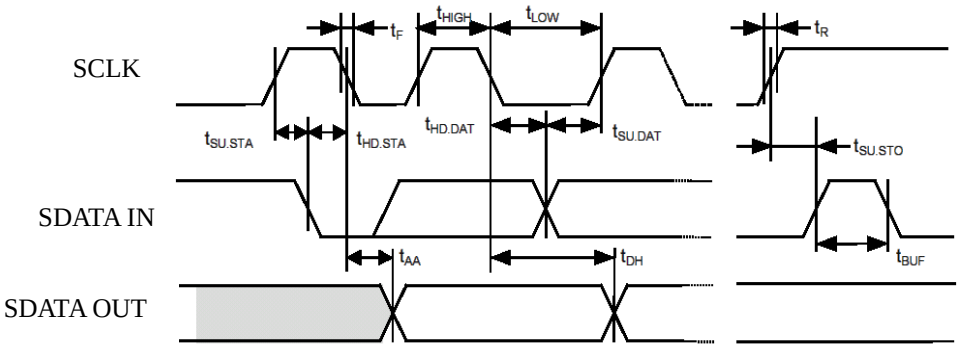
Note:

1. Full Scale (9999 counts for ADC)
2. ES222 built-in 3rd order low pass filter available for AC mode
3. Gain calibration is necessary for higher accuracy

AC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCLK clock frequency	f_{SCLK}	-	-	100	kHz
SCLK clock time "L"	t_{LOW}	4.7	-	-	us
SLCK clock time "H"	t_{HIGH}	4.0	-	-	
SDATA output delay time	t_{AA}	0.1	-	3.5	
SDATA output hold time	t_{DH}	100	-	-	ns
Start condition setup time	$t_{SU.STA}$	4.7	-	-	us
Start condition hold time	$t_{HD.STA}$	4.0	-	-	
Data input setup time	$t_{SU.DAT}$	200	-	-	ns
Data input hold time	$t_{HD.DAT}$	0	-	-	
Stop condition setup time	$t_{SU.STO}$	4.7	-	-	us
SCLK/SDATA rising time	t_R	-	-	1.0	
SCLK/SDATA falling time	t_F	-	-	0.3	
Bus release time	t_{BUF}	4.7	-	-	

MPU I/O timing diagram



Function Description

1. MPU serial I/O function overview

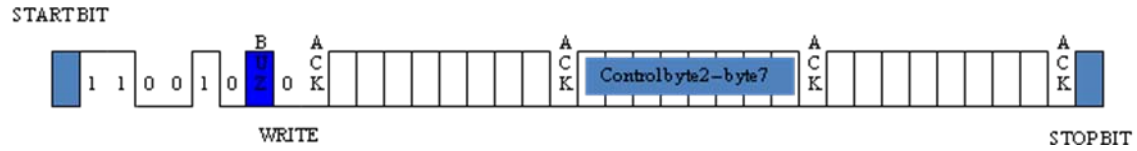
1.1 Introduction

ES222 configures a 3-wire serial I/O interface to external microprocessor unit (MPU). The SDATA pin is bi-directional and SCLK & DATANEW are unilateral. The SDATA pin is configured by open-drain circuit design. The DATANEW is used to check the data buffer of ADC ready or not. When the ADC conversion cycle is finished, the DATANEW pin will be pulled high until MPU send a valid read command to ES222. After the first ID byte is confirmed, the DATANEW will be driven to low until the next ADC conversion finished again.

The data communication protocol is shown below. The write protocol is configured by an ID byte with eight command bytes. The read protocol is configured by an ID byte with twelve data bytes.

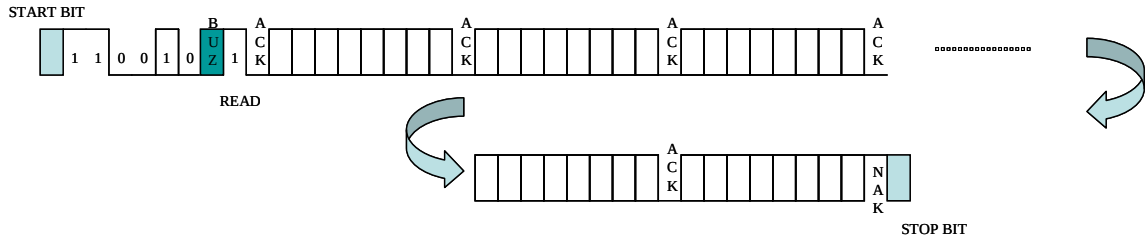
Write command:

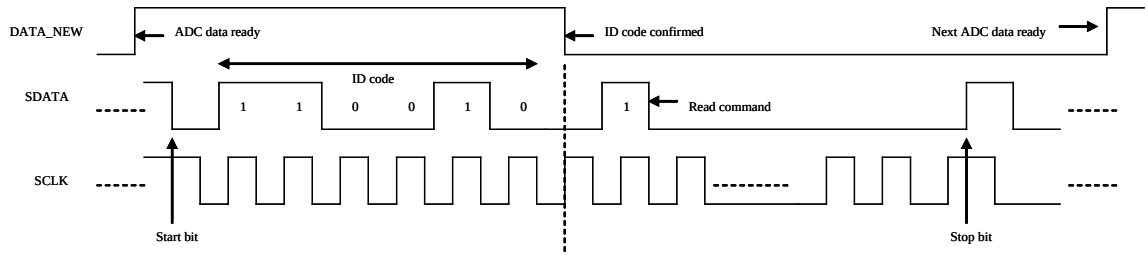
ID byte, Write control byte1 ~ control byte8



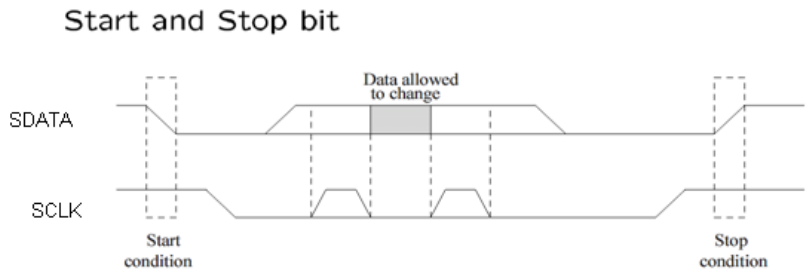
Read command:

ID byte, Read data byte1, Read data byte2 ~ Read data byte11, Read data byte12





The ID byte of ES222 is header of “110010” followed by a buzzer on/off control bit and R/W bit. The start/stop bit definition is shown on the diagram below.



1.2 Read/Write command description

The write command includes one ID byte with four command bytes. If the valid write ID code is received by ES222 at any time, the write command operation will be enabled.
The next table shows the content of write command: (ADC1/ADC2 controlled individually)

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID	1	1	0	0	1	0	**BUZ**	**R/W=0**
W1	F3	F2	F1	F0	C1_AD1	C0_AD1	C1_AD2	C0_AD2
W2	AC_1	AC_2	Q2	Q1	Q0	B2	B1	B0
W3	VAHZ_1	VAHZ_2	FQ2_1	FQ1_1	FQ0_1	FQ2_2	FQ1_2	FQ0_2
W4	PCAL_1	PCAL_2	PEAK_1	PEAK_2	AD12IN	AD21IN	AD1UPIN	AD2UPIN
W5	SUDP2_1	SUDP1_1	SUDP0_1	SUDP2_2	SUDP1_2	SUDP0_2	AD1OFF	AD2OFF
W6	LPF1_1	LPF0_1	LPF1_2	LPF0_2	0	UDPD10_1	0	UDPD10_2
W7	PHSEQ_1	PHSEQ_2	IOP1	IOP0	INA	FCOND	SHBP	0
W8	0	0	0	C_Clamp	R_FIN1M	DIOVSS	0	0

Buzzer driver ON/OFF control bit: **BUZ**

Measurement function control bit: **F3/F2/F1/F0**

ADC conversion rate selection: **C1_AD1/C0_AD1/C1_AD2/C0_AD2**

AC mode control enable bit: **AC_1/AC_2**

Range control bit for V/A/R/C modes: **Q2/Q1/Q0**

Buzzer frequency selection: **B2/B1/B0**

Frequency measurement for AC mode enabled control: **VAHZ_1/VAHZ_2**

Range control bit for FREQ mode: **FQ2_1/FQ1_1/FQ0_1/ FQ2_2/FQ1_2/FQ0_2**

Peak voltage detection offset calibration control bit: **PCAL_1/PCAL_2**

Peak hold measurement mode control bit: **PEAK_1/PEAK_2**

ADC1/ADC2 input channel MUX control: **AD12IN/AD21IN/AD1UPIN/AD2UPIN**

User-defined ADC1 input channel selection: **SUDP2_1/SUDP1_1/SUDP0_1**

User-defined ADC2 input channel selection: **SUDP2_2/SUDP1_2/SUDP0_2**

ADC disabled control**: AD1OFF/AD2OFF**

3dB BW for low-pass-filter selection: **LPF1_1/LPF0_1/LPF1_2/LPF0_2**

Full scale divided by ten for UDP mode control bit: **UDPD10_1/UDPD10_2**

3-phase voltage measurement at 1000V range of ADC1 or ADC2: **PHSEQ_1/PHSEQ_2**

OP configuration control bit: I**OP1/IOP0**

INRUSH measurement control: **INA**

Conductance mode enabled control at 10MΩ range: **FCOND**

Auxiliary low-resistance detection control bit for Continuity and Diode modes: **SHBP**

OVH1 path omitted control bit in Capacitance mode: **C_Clamp**

Frequency mode input terminal impedance: **R_FIN1M**

Diode measurement mode open source voltage selection: **DIOVSS**

ADC conversion rate selection: **C1_AD1/C0_AD1/C1_AD2/C0_AD2**

C1	C0	ADC Conversion Time	SADC Line noise rejection
0	0	350ms	50/60Hz
0	1	175ms	50/60Hz
1	0	87.5ms	60Hz
1	1	43.75ms	N/A

The read command includes one ID byte with 12 data bytes. When DATANEW is ready[1], MPU could send the read data command to get the result of both ADCs conversion (D0/D1/D2/D3)[2] or status flag from ES222. If the conversion rate of both ADCs is different, the status flag DRDY_D0/DRDY_D1 should be checked. If DRDY_D0=1, it means the D0 data is valid. If DRDY_D1=1, it means the D1 data is valid.

The next table shows the content of read command.

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID	1	1	0	0	1	0	**BUZ**	**R/W=1**
R1	HV_AD1	HV_AD2	ALARM	DRDY_D0	DRDY_D1	RPH	PMAX	PMIN
R2	Lduty	STA0_1	STA1_1	FIN_1	STA0_2	STA1_2	FIN_2	DISC
R3	LF1/INW	LF2/INF	SIGN_1	SIGN_2	D0:0	D0:1	D0:2	D0:3
R4	D0:4	D0:5	D0:6	D0:7	D0:8	D0:9	D0:10	D0:11
R5	D0:12	D0:13	D1:0	D1:1	D1:2	D1:3	D1:4	D1:5
R6	D1:6	D1:7	D1:8	D1:9	D1:10	D1:11	D1:12	D1:13
R7	D2:0	D2:1	D2:2	D2:3	D2:4	D2:5	D2:6	D2:7
R8	D2:8	D2:9	D2:10	D2:11	D2:12	D2:13	D2:14	D2:15
R9	D2:16	D2:17	D2:18	D2:19	D3:0	D3:1	D3:2	D3:3
R10	D3:4	D3:5	D3:6	D3:7	D3:8	D3:9	D3:10	D3:11
R11	D3:12	D3:13	D3:14	D3:15	D3:16	D3:17	D3:18	D3:19
R12	BTS0	BTS1	PHWAIT	LOCK	LEAD	LAG	PHTOUT	

[1]Note: DATANEW will be active when one ADC conversion finished. DATANEW for frequency or capacitance mode will be active when D0 or D3 data ready.

[2]Note: D0/D1/D2/D3 all are binary code format. D0 is ADC1 output and D1 is ADC2 output. The maximum data is 12000 counts for both ADCs.

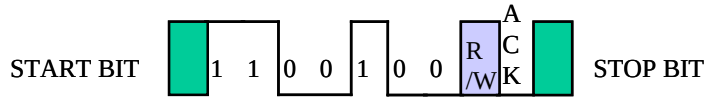
The ADC data output for measurement mode: **F3/F2/F1/F0**

F3	F2	F1	F0	Measurement mode	D0	D1	D2	D3
0	0	0	0	DCV+ACV	DCV	ACV		V_Hz
0	0	0	1	DCA+ACA	DCA	ACA		A_Hz
0	0	1	0	DCmV+ACmV	DCmV	ACmV		V_Hz
0	0	1	1	V or A dual	V	A	V_Hz	A_Hz
0	1	0	0	mV + A	mV	A	mV_Hz	A_Hz
0	1	0	1	V/A quad (AC+DC)	ACV	ACA	DCV/VHz	DCA/AHz
0	1	1	1	Resistance mode	Res.	UDP		
1	0	0	0	Continuity Mode	Cont.	UDP		
1	0	0	1	Capacitance mode	Cap.	UDP		
1	0	1	0	Diode mode	Diode	UDP		
1	0	1	1	LED mode	LED	UDP		
1	1	0	0	Hz + duty mode	Hz		Duty	Hz/Duty
1	1	0	1	UDP dual mode	UDP	UDP		Hz

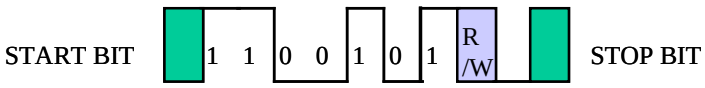
Buzzer frequency selection: **B2/B1/B0**

B2	B1	B0	Buzzer frequency
0	0	0	1.00kHz
0	0	1	2.67kHz
0	1	0	2.00kHz
0	1	1	3.33kHz
1	0	0	1.33kHz
1	0	1	3.08kHz
1	1	0	2.22kHz
1	1	1	4.00kHz

Set B2-B0 properly to get the target frequency. Use **BUZ** control bit to enable/disable the *BUZOUT* (pin91) driver output. If MPU control BUZ only, it is available to set ID byte with ending of stop bit.



Buzzer OFF



Buzzer ON

Status flags for measurement mode: ● = function available

Measurement mode	HV_n	ALARM	LDUTY	STA0_n	STA1_n	FIN_n	PMAX	PMIN
V mode		●					●	●
A mode	●						●	●
mV mode	●						●	●
VA dual mode	●	●	●	●	●	●	●	●
mVA dual mode	●		●	●	●	●	●	●
VA quad mode	●	●	●	●	●	●	●	●
mV quad mode	●		●	●	●	●	●	●
Res. mode	●							
Cont. mode	●	●						
Cap. mode	●	●						
Diode mode	●	●						
LED mode	●							
Hz+% mode	●	●	●	●	●	●		
UDP mode	●						●	●
Measurement mode	LF_n	INW/INF	SIGN_n	BTSn	PHWAIT	LOCK	DISC	RPH
V mode			●	●	●	●		
A mode		●	●	●				
mV mode			●	●				
VA dual mode	●	●	●	●	●	●		
mVA dual mode	●	●	●	●				
VA quad mode	●	●	●	●	●	●		
mVA quad mode	●	●	●	●				
Res. mode				●				●
Cont. mode				●				
Cap. mode				●			●	
Diode mode			●	●				
LED mode			●	●				
Hz+% mode	●			●				
UDP mode			●	●				

Description of status flags:

HV_1/HV_2: When abnormal voltage applied to ADC1/ADC2, the flag will be set.

ALARM: Status flag will be set when short detection in Cont./Diode mode or larger capacitance detection or higher frequency indication in Hz mode

DISC: Status flag for capacitor discharging mode

BTS0/BTS1: Multi-level battery voltage indication

LF_1/LF_2: Lower frequency indication for Hz mode of ADC1/ADC2

LDUTY: Low duty indication for Hz + duty mode

STA0_1/STA1_1/STA0_2/STA1_2: divider indication for Hz mode of ADC1/ADC2.

FIN_1/FIN_2: Measurement cycle finished for Hz mode of ADC1/ADC2

PMAX: Indicate the ADC data (D0 or D1) is the output of peak maximum voltage

PMIN: Indicate the ADC data (D0 or D1) is the output of peak minimum voltage

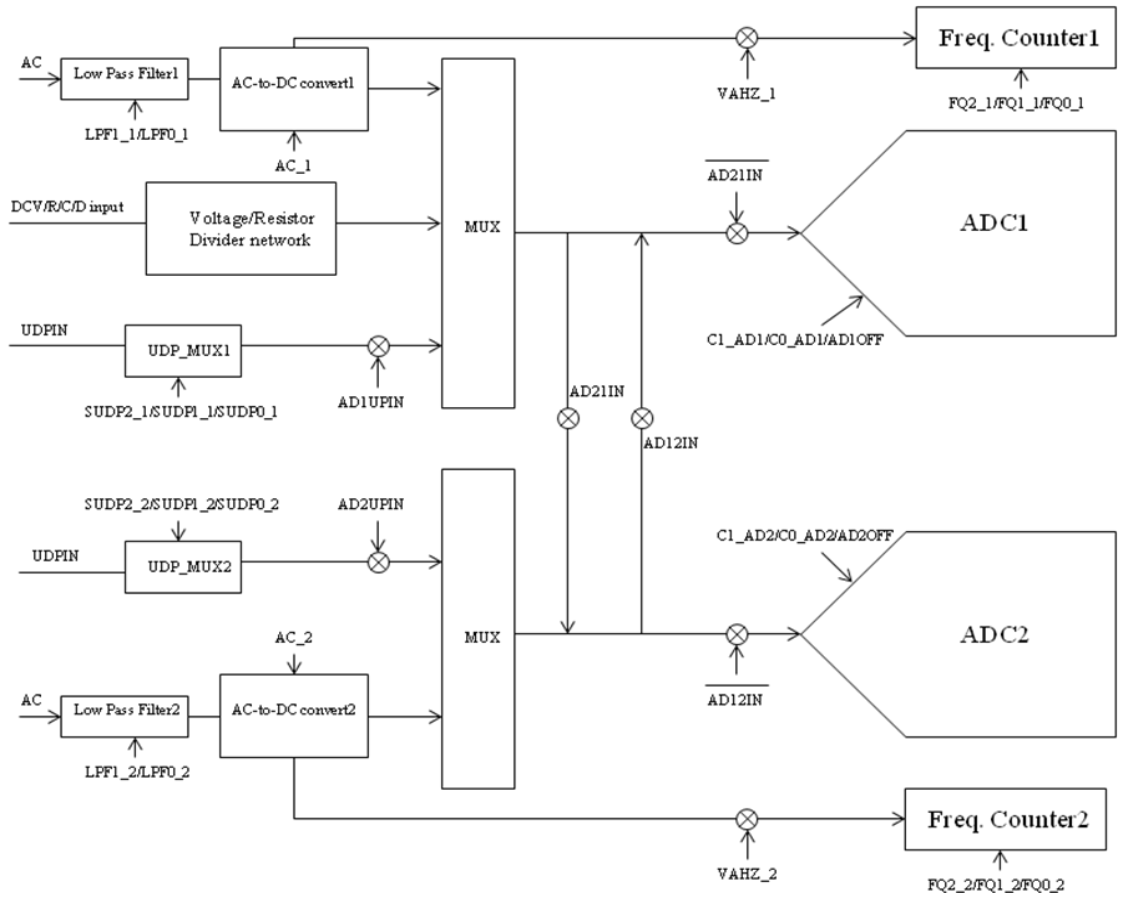
PHWAIT/PHTOUT: Waiting or timeout status indication for 3-phase detection

LOCK/LEAD/LAG: Phase detection status indication for 3-phase detection

RPH: ADC output indication bit for conductance mode

INW/INF: Status flag indication for ACA inrush mode

1.3 Function Block Diagram



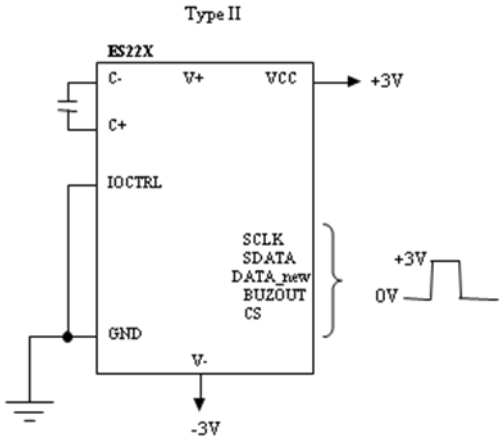
ES222 includes dual ADC core which could be controlled individually. **C1/C0** set the ADC conversion rate. The both ADCs could be set in different conversion rate. ES222 is implemented by resistor divider network to decrease external complex analog switches for DMM application. It also includes UDP channels to implement current mode network or other special measurement mode. The input channels could be DC signals or from output of AC-to-DC converter (AC mode is active). It also could be switched another path to frequency counter if VAHZ control mode is active. If AD1OFF or AD2OFF is set to high, the ADC1 or ADC2 core will enter power down mode, respectively.

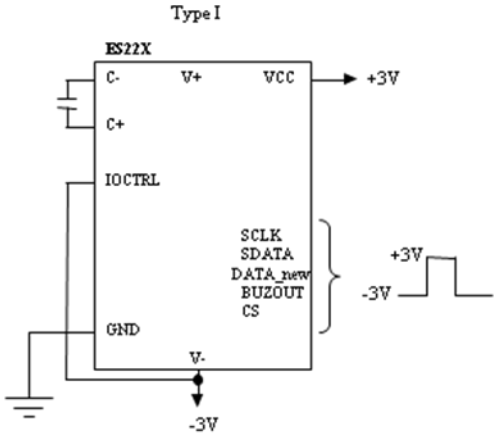
ADC1/ADC2 input channel MUX control: **AD12IN/AD21IN/AD1UPIN/AD2UPIN**

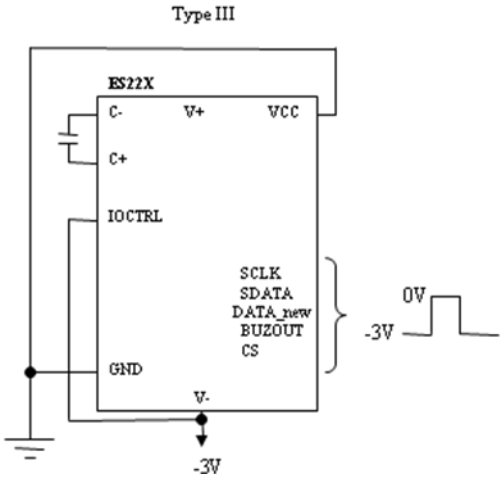
Set control bit = 1	Description
AD12IN	ADC1 input switched to ADC2 input channel simultaneously
AD21IN	ADC2 input switched to ADC1 input channel simultaneously
AD1UPIN	ADC1 input switched to UDPIN input channel (selected by SUDPn_1)
AD2UPIN	ADC2 input switched to UDPIN input channel (selected by SUDPn_2)

1.4 Power & I/O level selection

The ES222 provide a flexible I/O level setting for different MPU system configuration. The VCC should be connected to the same potential of external Vcc of MCU. The VCC is allowed to be set between DGND ~ V+. The IOCTRL pin selects the Vss level of MCU. If IOCTRL is set to DGND, the Vss level of MCU is the same as DGND. If IOCTRL is set to V-, the Vss level of MCU is the same as V-.







2. Operating Modes

2.1. DC+AC Voltage Measurement

MPU send write command to select the DC+AC voltage measurement function. The Hz mode measurement is available to be enabled by setting **VAHZ_2**=1 simultaneously. The measured signal is applied to *VR1* terminal (pin21) through 10MΩ or applied to *mVin* terminal (pin23) if mV range mode is selected by MPU command.

See the next table of function command:

F3	F2	F1	F0	Measurement mode	Read data bytes
0	0	0	0	DCV + ACV mode	D0(0:13), D1(0:13), D3(0:19)
0	0	1	0	DCmV+ACmV mode	D0(0:13), D1(0:13), D3(0:19)

Note: D0/D1/D3 all are binary format. SIGN_1 & SIGN_2 are the sign bit of D0/D1, respectively.

Range control for voltage mode (DCV+ACV)

Q2	Q1	Q0	Full Scale Range	Divider Ratio	Resister Connection
0	0	0	.9999V	1/10	VR2 (1.111MΩ)
0	0	1	9.999V	1/100	VR3 (101kΩ)
0	1	0	99.99V	1/1000	VR4 (10.01kΩ)
0	1	1	999.9V	1/10000	VR5 (1kΩ)

Range control for mV mode (DCmV+ACmV)

Q2	Q1	Q0	Full Scale Range	Input terminal
0	0	0	99.99mV	*mVin*
0	0	1	600.0mV*	*mVin*

Note: AC/DC 600mV range is necessary to do additional gain calibration.

Frequency range control for ACV mode (set **VAHZ_2**=1)

FQ2_2	FQ1_2	FQ0_2	Full Scale Range
0	0	0	99.99Hz
0	0	1	999.9Hz
0	1	0	9.999kHz
0	1	1	99.99kHz

Note: See frequency/duty mode (section 2.10) also

2.2 DC+AC Current measurement

MPU send write command to select the DC+AC current measurement function. The Hz mode measurement is available to be enabled by setting **VAHZ_2**=1 simultaneously.
See the next table of function command:

F3	F2	F1	F0	Measurement mode	Read data bytes
0	0	0	1	DCA + ACA mode	D0(0:13), D1(0:13), D3(0:19)

Note: D0/D1/D3 all are binary format. SIGN_1 & SIGN_2 are the sign bit of D0/D1, respectively.

The external current sensed signal is applied to *UDP* terminals (pin24-25,27-28,30-31,33). The input channel is selected by write command as following: (Use multiple terminals to implement auto range scheme)

SUDP2_n[1]	SUDP1_n[1]	SUDP0_n[1]	Full Scale Range[2]	Input terminals
0	0	0	99.99mV	UDPIN1
0	0	1	99.99mV	UDPIN2
0	1	0	99.99mV	UDPIN31
0	1	1	99.99mV	UDPIN32
1	0	0	99.99mV	UDPIN41
1	0	1	99.99mV	UDPIN42
1	1	0	99.99mV	UDPIN5

[1]Note: n should be 1 & 2 simultaneously.
[2]Note: Full scale range could be changed from 99.99 to 999.9mV when UDPD10_n=1.

Frequency range control for ACA mode (set **VAHZ_2**=1)

FQ2_2	FQ1_2	FQ0_2	Full Scale Range
0	0	0	99.99Hz
0	0	1	999.9Hz
0	1	0	9.999kHz
0	1	1	99.99kHz

Note: See frequency mode (section 2.10) also.

2.3 Low pass filter (LPF) mode for ACA/ACV mode

A 3rd order low pass filter with is built in ES222. The 3dB bandwidth of the low pass filter could be selectable by MPU. The LPF mode is enabled when the LPF control bit is set to be active. The low pass filter control bit could be set individually for ADC1 or ADC2
.

LPF1_n	LPF0_n	Low pass filter effect
0	0	Disable
0	1	3dB = 1kHz
1	0	3dB = 10kHz
1	1	3dB > 100kHz

Note: n = 1 or 2

2.4 mV or V/A dual mode measurement

MPU send write command to select the voltage/current dual measurement function. The voltage & current sensed signal could be applied into meter simultaneously. The Hz mode measurement is available to be enabled by setting **VAHZ_1**=1 / **VAHZ_2**=1. The voltage measured signal is applied to *VR1* terminal (pin21) through 10MΩ in V/A dual mode. The voltage measure signal is applied to *mVin* terminal(pin26) in mV/A dual mode.

F3	F2	F1	F0	AC_1	AC_2	Measurement mode	Read data bytes
0	0	1	1	0	0	DCV+DCA mode	D0(0:13), D1(0:13), D2(0:19), D3(0:19)
0	0	1	1	1	1	ACV+ACA mode	D0(0:13), D1(0:13), D2(0:19), D3(0:19)
0	1	0	0	0/1	0/1	mV + A mode	D0(0:13), D1(0:13), D2(0:19), D3(0:19)

Note: D0/D1/D2/D3 all are binary format. SIGN_1 & SIGN_2 are the sign bit of D0/D1, respectively.

Range control for voltage mode (DCV or ACV)

Q2	Q1	Q0	Full Scale Range	Divider Ratio	Resister Connection
0	0	0	.9999V	1/10	VR2 (1.111MΩ)
0	0	1	9.999V	1/100	VR3 (101kΩ)
0	1	0	99.99V	1/1000	VR4 (10.01kΩ)
0	1	1	999.9V	1/10000	VR5 (1kΩ)

Range control for mV mode

Q2	Q1	Q0	Full Scale Range	Input terminal
0	0	0	99.99mV	*mVin*
0	0	1	600.0mV*	*mVin*

Note: AC/DC 600mV range is necessary to do additional gain calibration.

The external current sensed signal is applied to *UDP* terminals (pin24-25,27-28,30-31,33). The input channel is selected by write command as following: (It is possible to use multiple terminals to implement auto range scheme)

SUDP2_2	SUDP1_2	SUDP0_2	Full Scale Range*	Input terminals
0	0	0	99.99mV	UDPIN1
0	0	1	99.99mV	UDPIN2
0	1	0	99.99mV	UDPIN31
0	1	1	99.99mV	UDPIN32
1	0	0	99.99mV	UDPIN41
1	0	1	99.99mV	UDPIN42
1	1	0	99.99mV	UDPIN5

Note: Full scale range could be changed by UDPD10_2.

Frequency range control for ACV or ACA mode (set **VAHZ_1**=1 / **VAHZ_2**=1)

FQ2_N	FQ1_N	FQ0_N	Full Scale Range
0	0	0	99.99Hz
0	0	1	999.9Hz
0	1	0	9.999kHz
0	1	1	99.99kHz

Note1: See frequency/duty mode (section 2.10) also

Note2: N should be 1 or 2 depends on whether VAHZ_1 or VAHZ_2 is set or not.

2.5 V/A quad mode measurement

MPU send write command to select the voltage/current quad measurement function. The AC+DC voltage & AC+DC current sensed signal could be applied into different terminal simultaneously. The Hz mode measurement is available to be enabled by setting **VAHZ_1**=1 or **VAHZ_2**=1. The measured voltage signal is applied to *VR1* terminal (pin21) through 10MΩ.

F3	F2	F1	F0	Measurement mode	Read data bytes
0	1	0	1	V/A Quad mode	D0(0:13), D1(0:13), D2(0:19), D3(0:19)

Note: D0/D1/D2/D3 all are binary format. SIGN_1 & SIGN_2 are the sign bit of D2/D3, respectively.

Range control for voltage mode (DCV+ACV)

Q2	Q1	Q0	Full Scale Range	Divider Ratio	Resister Connection
0	0	0	.9999V	1/10	VR2 (1.111MΩ)
0	0	1	9.999V	1/100	VR3 (101kΩ)
0	1	0	99.99V	1/1000	VR4 (10.01kΩ)
0	1	1	999.9V	1/10000	VR5 (1kΩ)

The external current sensed signal is applied to *UDP* terminals (pin24-25,27-28,30-31,33). The input channel is selected by write command as following: (Use multiple terminals to implement auto range scheme)

SUDP2_n[1]	SUDP1_n[1]	SUDP0_n[1]	Full Scale Range[2]	Input terminals
0	0	0	99.99mV	UDPIN1
0	0	1	99.99mV	UDPIN2
0	1	0	99.99mV	UDPIN31
0	1	1	99.99mV	UDPIN32
1	0	0	99.99mV	UDPIN41
1	0	1	99.99mV	UDPIN42
1	1	0	99.99mV	UDPIN5

[1]Note: n = 1 or 2.

[2]Note: Full scale range could be changed from 99.99 to 999.9mV when UDPD10_n=1.

Frequency range control for ACV or ACA mode (set **VAHZ_1**=1 or **VAHZ_2**=1)

FQ2_N	FQ1_N	FQ0_N	Full Scale Range
0	0	0	99.99Hz
0	0	1	999.9Hz
0	1	0	9.999kHz
0	1	1	99.99kHz

Note: See frequency/duty mode (section 2.10) also

Note2: N should be 1 or 2 depends on whether VAHZ_1 or VAHZ_2 is set or not.

2.6 Resistance/Conductance Measurement

MPU send write command to select the resistance measurement function.

F3	F2	F1	F0	Measurement mode	Read data bytes
0	1	1	1	Resistance mode	D0(0:13), D1(0:13)

Note1: D0/D1 both are binary format. SIGN_2 is the sign bit of D1. Resistance value is D0

Note2: If AD2UPIN=1, D1 data is the ADC result of *UDP* terminals.

Range control for resistance mode

Q2	Q1	Q0	Full Scale Range	Relative Resistor	Equivalent value
0	0	0	99.99Ω	OR1	100Ω
0	0	1	999.9Ω	VR5	1KΩ
0	1	0	9.999KΩ	VR4 ‖ VR1	10KΩ
0	1	1	99.99KΩ	VR3 ‖ VR1	100KΩ
1	0	0	999.9KΩ	VR2 ‖ VR1	1MΩ
1	0	1	9.999MΩ	VR1	10MΩ
1	1	0	99.99MΩ	VR1	10MΩ

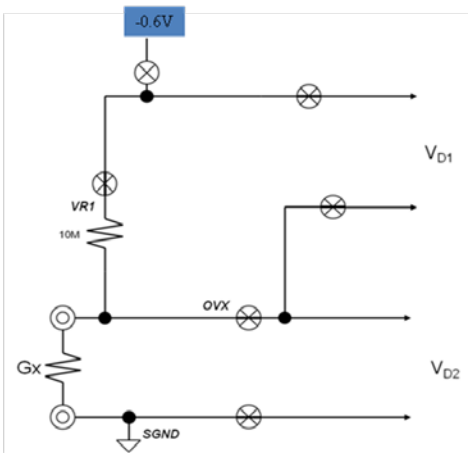
Set **FCOND**=1 when range control is 10MΩ range, the conductance mode is available. The status RPH bit is used for converted data indication of reference voltage or input voltage.

Q2	Q1	Q0	Full Scale Range	Relative Resistor	Equivalent value
1	0	1	199.9nS	VR1	10MΩ

The maximum displayed count is 2000 and the resolution should be 0.1nS. The MCU should check the status bit RPH and D0 simultaneously. When RPH=1 the D0 data should be V_{D1}. If RPH=0, then the D0 data should be V_{D2}. The DUT conductance value could be calculated by simple formula.

Conductance mode 199.9nS

$Gx = V_{D1}/V_{D2} * 1000$



2.7 Capacitance Measurement

MPU send write command to select the capacitance measurement function.

F3	F2	F1	F0	Measurement mode	Read data bytes
1	0	0	1	Capacitance mode[3]	D0(0:13), D1(0:13)

Note1: D0/D1 both are binary format. SIGN_2 is the sign bit of D1. Capacitance value is D0

Note2: If AD2UPIN=1, D1 data is the ADC result of *UDP* terminals.

Range control for capacitance mode

Q2	Q1	Q0	Full Scale Range	Relative Resistor	Measurement Period
0	0	0	9.999nF	-	0.45 sec
0	0	1	99.99nF	OVX pin VR	0.45 sec
0	1	0	999.9nF		1.2 sec max.
0	1	1	9.999uF	R9K / R1K	1.4 sec max.
1	0	0	99.99uF[2]	R9K / R1K	1.4 sec max.
1	0	1	999.9uF	R9K / R1K	2.5 sec max.
1	1	0	9.999mF[1]	R9K / R1K	2.5 sec max.
1	1	1	99.99mF[1]	R9K / R1K	25 sec max.

[1]**Note**: The displayed counts in ES222 capacitance mode is recommended to be divided by 10 for range larger then 1mF. (1000 counts displayed is recommended)

[2]**Note**: ALARM bit at capacitance mode is used for increasing the ranging speed. If MPU check the ALARM=1 at lower range, it could set the next range to 99.99uF directly and the ADC output should be ignored.

[3]**Note**: DISC status bit is used for detection of DUT capacitor voltage. If DISC=1, the internal capacitor discharging mode is active and the capacitance measurement is inhibited. It is recommended to discharge the DUT capacitor externally.

[4]**Note**: Set **C_Clamp**=1 to reduce the internal charging current with higher resistance allowed for *OVH/OVH1* paths. In this case, *OVH1* path could be ignored.

2.8 Continuity Check

MPU send write command to select the continuity measurement function.

F3	F2	F1	F0	Measurement mode	Read data bytes
1	0	0	0	Continuity mode	D0(0:13), D1(0:13)

Note1: D0/D1 both are binary format. SIGN_2 is the sign bit of D1. Resistance value is D0.

Note2: If AD2UPIN=1, D1 data is the ADC result of *UDP* terminals.

Continuity mode shares the same configuration with 99.99Ω resistance measurement circuit and support the low-resistance detection. If the *STBEEP* output (pin83) is low, it means the low-resistance status is detected (It means the *OVX* terminal voltage less than -7mV). It could be faster than the ADC1 result, so MPU could monitor the *STBEEP* output and ADC1 (D0) data output make the high speed detection for short circuit detection. Set **SHBP**=1 to enable the built-in buzzer driving automatically when *STBEEP* is active.

2.9 Diode/LED mode Measurement

MPU send write command to select the diode or LED measurement function.

F3	F2	F1	F0	Measurement mode	Read data bytes
1	0	1	0	Diode mode	D0(0:13), D1(0:13)
1	0	1	1	LED mode	D0(0:13), D1(0:13)

Note1: D0/D1 both are binary format. SIGN_1 & SIGN_2 are the sign bit of D0/D1, respectively. Diode voltage value is D0.

Note2: If AD2UPIN=1, D1 data is the ADC result of *UDP* input terminals.

Diode measurement mode shares the same configuration with 9.999V voltage measurement circuit and support the low-resistance detection. If the *STBEEP* output (pin83) is low, it means the low-resistance status is detected (It means the *OVX* terminal voltage less than 9mV). It could be faster than the ADC1 result, so MPU could monitor the *STBEEP* output and ADC1 (D0) data output make the high speed detection for short circuit detection. Set **SHBP**=1 to enable the built-in buzzer driving automatically when *STBEEP* is active. The default source voltage at diode mode is the same as V+ potential. Set **DIOVSS**=1 when diode measurement to change source voltage from V+ to V- potential.

Because some LED device will need higher voltage source to turn on, so MPU could select LED mode to change the source voltage to external source. The external voltage source (positive or negative) applied from rotary switch.

2.10 Frequency/duty cycle mode measurement

MPU send write command to select the frequency mode measurement. Set **R_FIN1M** =1 to change the impedance of frequency input terminal from 100KΩ to 1MΩ around.

F3	F2	F1	F0	Measurement mode	Read data bytes
1	1	0	0	Hz/ Duty mode	D0(0:13), D1(0:13), D2(0:19), D3(0:19)

Note1: D0/D1/D2/D3 all are binary format. SIGN_1 & SIGN_2 are the sign bit of D0/D1, respectively.

Note2: If AD2UPIN=1, D1 data is the ADC result of *UDP* terminals.

Range control for frequency mode

FQ2_1	FQ1_1	FQ0_1	Full Scale	Conversion period
0	0	0	99.99Hz	350ms (fixed)
0	0	1	999.9Hz	350ms (fixed)
0	1	0	9.999KHz	350ms (fixed)
0	1	1	99.99KHz	350ms (fixed)
1	0	0	999.9KHz	350ms (fixed)
1	0	1	9.999MHz	350ms (fixed)
1	1	0	40.00MHz	350ms (fixed)

Available minimum frequency input F_{MIN} = 1.00Hz

Hz & duty cycle mode computed by D0/D2/D3 (If status flag FIN=1)

Flag	**STA0[1]=1**	**STA0[1]=0**	
Range		**STA1[1]=1**	**STA1[1]=0**
99.99Hz	FREQ=100000000/D3[3]	FREQ=400000000/D3[3]	FREQ=1600000000/D3[3]
999.9Hz	FREQ=10000000/D3[3]	FREQ=80000000/D3[3]	FREQ=640000000/D3[3]
9.999KHz	FREQ=1000000/D3[3]	FREQ=4000000/D3[3]	FREQ=256000000/D3[3]
99.99KHz	FREQ = ADC counter (D0)[2]		
999.9KHz			
9.999MHz			
40.00MHz			

[1]Note: If Hz+duty mode is selected or VAHZ_1 is set to active, assign STA0= STA0_1 & STA1=STA1_1 & FIN=FIN_1. If VAHZ_2 is set to active, assign STA0= STA0_2 & STA1=STA1_2 & FIN=FIN_2.

[2]Note: If VAHZ_1 is active, ADC counter will be D2. If VAHZ_2 is active, ADC counter will be D3.

[3]Note: If VAHZ_1 is active, D3 should be replaced by D2.

Status Flag	LDUTY=1	LDUTY=0
Duty cycle (<10kHz)	10000-D2*10000/D3	D2*10000/D3

Note: 5.0%~95.0% , 0.1% resolution is recommended.

The status flag FIN indicate the frequency input signal available (> F_{MIN}) or not. If the computed result less than F_{MIN}, the frequency/duty cycle readings should be set to zero.

The status flags ALARM & LF are used for fast judgment of proper range. If frequency input is larger than 12.5 kHz, ALARM will be active. If frequency input is floating or frequency detected too low, LF will be active.

Auto range consideration for MPU by using Status Flags of frequency mode

<table>
<tr><th>Flag
Range</th><th>FIN=0</th><th>FIN=0 or 1</th><th colspan="2">FIN=1</th></tr>
<tr><th></th><th>LF=0</th><th>LF=1*</th><th>ALARM=LF=0</th><th>ALARM=1**</th></tr>
<tr><td>99.99Hz
999.9Hz
9.999KHz</td><td rowspan="2">Data and Range is not necessary to be updated</td><td>Hz/Duty=0</td><td rowspan="2">Change range depends on data computed</td><td>Set range to 99.99kHz range</td></tr>
<tr><td>99.99KHz
999.9KHz
9.999MHz
40.00MHz</td><td>Set range to 99.99Hz range</td><td>Change range depends on data computed</td></tr>
</table>

*Note: LF=1 @ 60Hz range implies the frequency is not available to be measured. The Hz/Duty readings should be set to zero.

**Note: When VAHZ mode is selected, the ALARM status should be ignored. Change range depends on data calculation result.

Duty cycle mode range (Input sensitivity > 2Vpp @ duty cycle = 5.0% & 95.0%)

Freq. range	Duty range*
99.99Hz 999.9Hz	5.0% - 95.0%
9.999KHz	10.0 % - 90.0%

2.11 UDP dual mode

MPU send write command to select the UDP mode measurement function. The signal full scale is 100mV for DC/AC mode. The UDPD10_1/UDPD10_2 control bits set the full scale from 100mV to 1V. The AC_1/AC_2 control bits set the AC mode. The VAHZ_1/VAHZ_2 control bits set the Hz mode.

See the next table of function command:

F3	F2	F1	F0	Measurement mode	Read data bytes
1	1	0	1	UDP dual mode	D0(0:13), D1(0:13), D2(0:19), D3(0:19)

Note: D0/D1/D2/D3 all are binary format. SIGN_1 & SIGN_2 are the sign bit of D0/D1, respectively.

The measured signal is applied to *UDP* terminals (pin24-25,27-28,30-31,33). The input channel is selected by write command as following:

SUDP2_n*	SUDP1_ n*	SUDP0_ n*	Input terminals
0	0	0	UDPIN1
0	0	1	UDPIN2
0	1	0	UDPIN31
0	1	1	UDPIN32
1	0	0	UDPIN41
1	0	1	UDPIN42
1	1	0	UDPIN5

Note:

1. When n=1, the input terminal will be set to ADC1 (D0). When n=2, the input terminal will be set to ADC2 (D1).

2. The reference voltage is taken from VA_UDPN terminals, which N is 1 to 5.

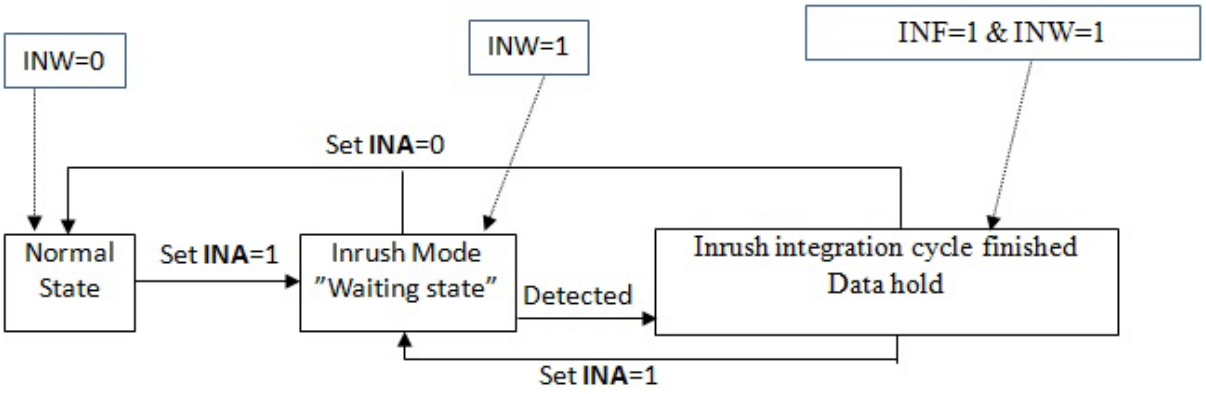
Frequency range control for AC mode (set **VAHZ_1**=1 or **VAHZ_2**=1)

FQ2	FQ1	FQ0	Full Scale Range
0	0	0	99.99Hz
0	0	1	999.9Hz
0	1	0	9.999kHz
0	1	1	99.99kHz

Note: See frequency/duty mode (section 2.10) also

2.2 Inrush measurement

ES222 provides an inrush function for AC current measurement of clamp-on meter to dectect the starting-up current of a motor. Only ACA/UDP(AC) modes support inrush measurement mode. SET control bit **INA**=1 of write command to enter the inrush function. Initially, the status bit INW=1 means to wait for signal triggered (Vpp > 14mV typ.). If the external starting-up signal is applied and detected, ES222 will execute the inrush measurement. When the inrush measurement is finished, the status bit INF=1 to indicate the inrush integration cycle is finished. It means the ADC2 data (D1) is ready to access by MCU. To enter inrush mode cycle again, set control bit **INA**=1 of write command and repeat the procedures mentioned above. To exist inrush mode, set **INA**=0 of write command. For INRUSH function, an external **true RMS-to-DC ES5 IC** is required. The flow chart of inrush function is shown below.



2.3 Peak-hold measurement mode

ES222 provides a peak hold function to capture the real peak value for voltage or current measurement mode. In a case of a 1V sine wave input voltage, the peak hold function gets a maximum peak value of 1.414V and minimum peak value of –1.414V ideally. Set the control bit **PEAK_1=1 or PEAK_2 =1** to force the ES222 entering PEAK hold measurement mode for ADC1 (D0) or ADC2 (D1). The PEAK_1 & PEAK_2 are not allowed to set simultaneously. Peak Hold function is divided into three parts of peak maximum, peak minimum & current RMS conversion. The ADC performs peak maximum / current value and peak minimum / current value conversion sequentially, not at the same time. The status flag PMAX or PMIN shows that type of the peak value. If PMAX=1(PMIN=1), the ADC output (D0 or D1) is the conversion data on *PMAX (PMIN)* terminals (pin 72/73). The MPU should make the comparison procedure to get the maximum value of *PMAX* data and minimum value of *PMIN* data. If PMAX=0 & PMIN=0, that means ADC is the current RMS value conversion result.

Peak calibration mode

At PEAK-Hold measurement mode, the offset voltage of internal operation amplifier will cause an error. To obtain a more accurate value, the offset error must be canceled. ES222 provides the peak calibration feature to remove the influence on accuracy by internal offset voltage. Set the control bit **PCAL**=1 to enter peak calibration mode. When PCAL mode is active, the ADC of ES222 will output the calibration value of peak maximum and minimum conversion in turn. The offset values should be memorized respectively and deducted from the data of *PMAX/PMIN* at the normal peak measurement mode. (PMAX = VPMAX_current_value – VPMAX_offfset & PMIN = VPMIN_current_value – VPMIN_offset)

Set PEAK=1 or PCAL=1		
Status indication	**PMAX=1, PMIN=0**	**PMAX=0, PMIN=1**
ADC data	$V_{PMAX.C}$	$V_{PMIN.C}$

$V_{PMAX.C}$ and $V_{PMIN.C}$ are not the real-time value of peak-hold voltage. They are the voltage stored on terminal capacitor (pin72-73). Because the capacitor will be self-discharging, so MCU need to compare the $V_{PMAX.C}$ & $V_{PMIN.C}$ respectively and memorize the maximum and minimum peak values in turn.

2.4 Phase Rotation

The ES222 provide the phase rotation to find the phase sequence of 3-phase of power source. The function will be available only at ACV 1000.0V range. When PHSEQ_1 or PHSEQ_2 is set active for ACV mode, the ACV measurement for ADC1 or ADC2 will be still kept in process. The PHWAIT status flag will be indicated and the phase rotation measurement is active. Start to measure any 2 terminals (named ***A/B***) of 3-phase voltage source. If the status flag (LOCK) is set and ACV_RMS is larger than 80V & AC frequency should be within 40~80Hz, the reference phase lock is confirmed. Then fix one terminal measured (named A) and change another one of measured terminals (named ***B***) **within 5 seconds** to the third terminal (named ***C***) which has been not measured. The ES222 will calculate the phase-shift between both measurements. Then the status flag of LEAD or LAG will be set respectively. If LEAD=1, the phase sequence is ***C→B→A***. If LAG=1, the phase sequence is ***A→B→C.*** If the status flag PHTOUT is set after 5 seconds, the whole operation should be reset again (Set PHSEQ=1 again). To exit phase rotation mode, set PHSEQ=0 of write command.

2.5 Sleep

Set *CS* pin (pin 78) to logic low to make the ES222 entering the sleep mode. The current consumption will be less than 15uA typically. Set *CS* pin to logic high or kept floating, the ES222 will return to normal operation.

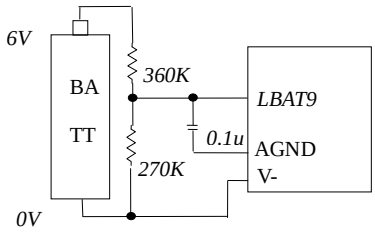
2.6 Multi-level battery voltage indication

The ES222 is built-in a comparator for batter voltage indication. The voltage is applied to *LBAT9* pin (pin 111) vs. *V-* terminal. MPU could check the status bit BTS1/BTS0 and monitor the *LBAT9* voltage status.

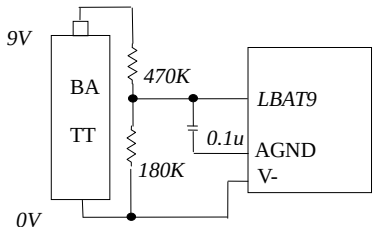
Battery voltage	BTS1	BST0
$V_{LBT} > V_{t1}$	1	1
$V_{t2} < V_{LBT} < V_{t1}$	1	0
$V_{t3} < V_{LBT} < V_{t2}$	0	1
$V_{LBT} < V_{t3}$	0	0

Low battery configuration for 9V/1.5V*4/1.5V*3 battery

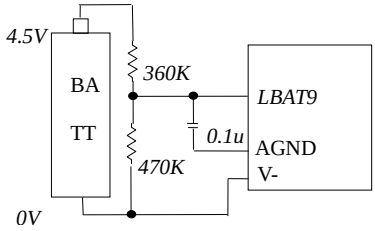
Low battery test circuit (a)



Low battery test circuit (b)



Low battery test circuit (c)



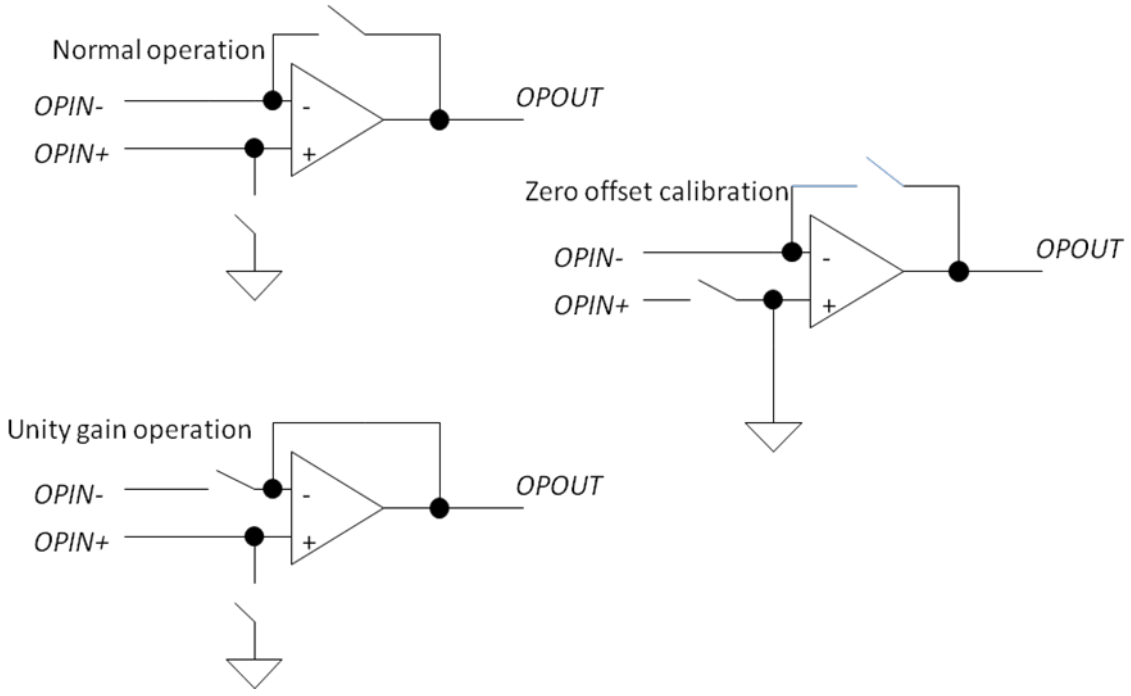
2.7 Independent OPAMP

ES222 is built-in an independent OPAMP with low drift offset using for general purpose.

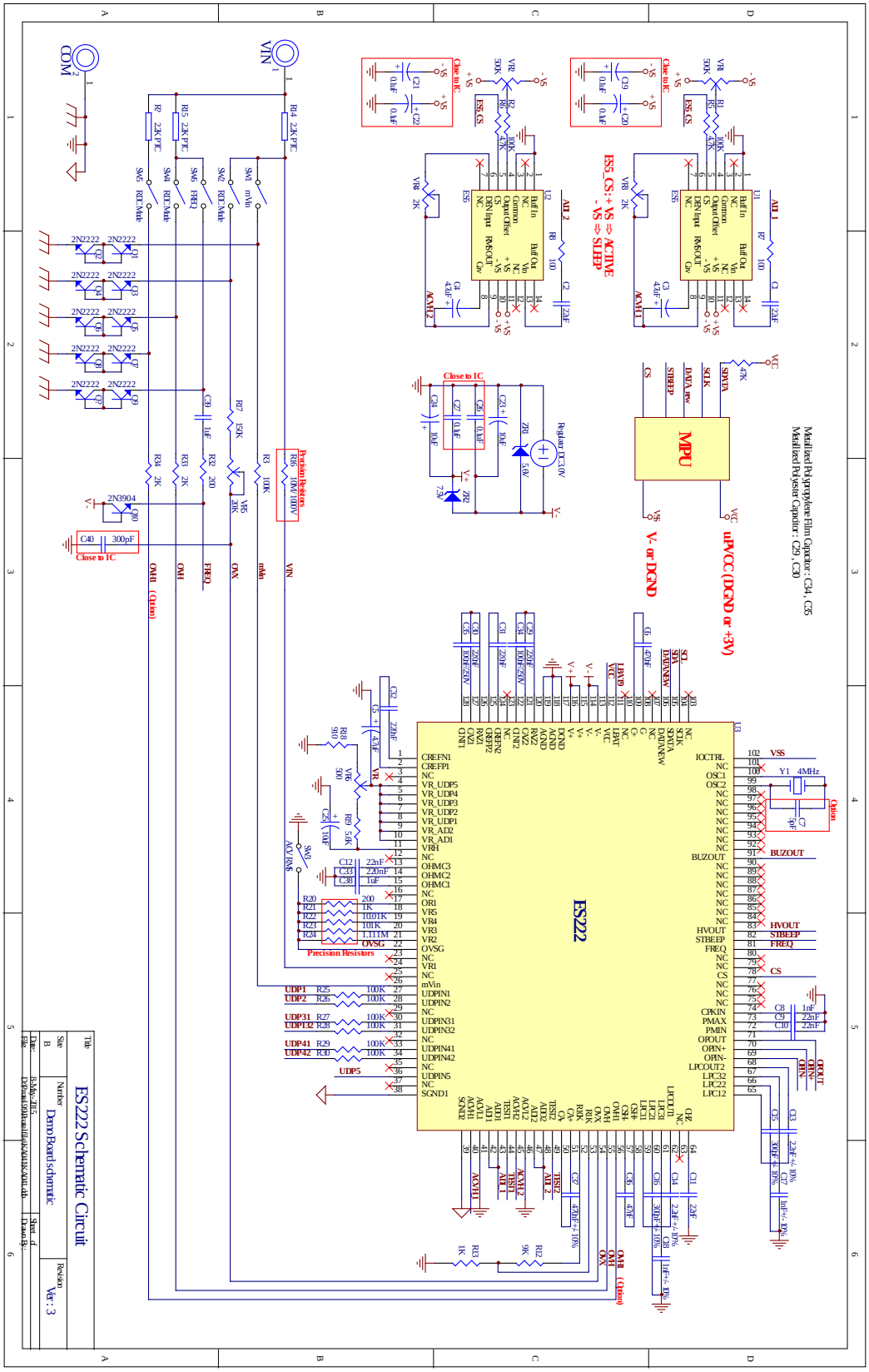
MPU could control the OP1/OP0 to change the OPAMP configuration:

IOP1	IOP0	OPAMP configuration
0	0	OPAMP OFF
0	1	Normal
1	0	Unity gain buffer
1	1	Zero calibration

Independent OPAMP configuration

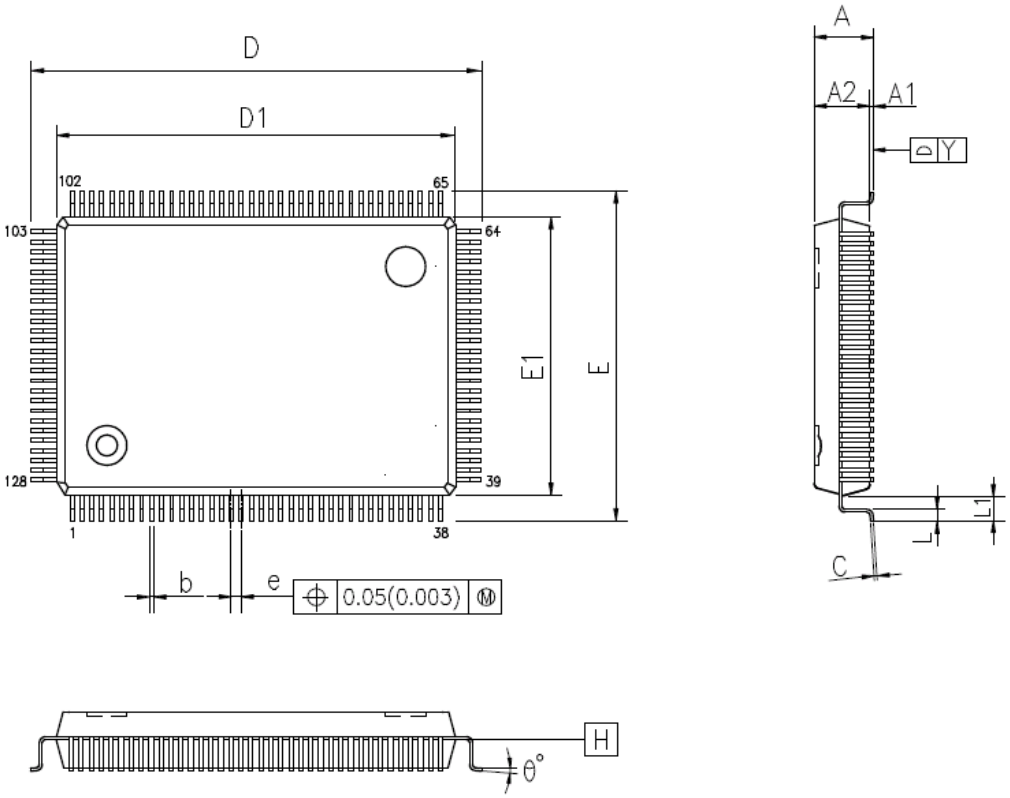


3. Application Circuit



4. Package Information

4.1 128L LQFP Outline drawing



4.2 Dimension parameters

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
C	0.10	0.15	0.20
D1	–	20.00 BSC	–
E1	–	14.00 BSC	–
e	–	0.50 BSC	–
D	–	22.00 BSC	–
E	–	16.00 BSC	–
L	0.45	0.60	0.75
L1	–	1.00 REF	–
Y	–	–	0.08
θ°	0°	3.5°	7°

UNIT : mm

NOTES:
1.JEDEC OUTLINE:
MS-026 BHB.
MS-026 BHB-HD(THERMALLY ENHANCED VARIATIONS ONLY).
2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS E1 AND D1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS E AND E DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .