

# ES166 LCR/DMM analog front

# Features

- Built-in 6000 counts dual slope ADC
- LQFP-80L package
- 3V DC power supply
- Support digital multi-meter function
  \*Voltage measurement (AC/DC) (600mV-1000V)
  \*Current measurement (AC/DC) (2-range auto)
  \*Dual mode for frequency with voltage or current
  \*DC Resistance measurement (600.0Ω 60.00MΩ)
  \*Diode or continuity mode measurement
  \*Logic frequency counter with duty cycle display:
  600.0Hz 20.00MHz
  - 5% 95%
- ADP mode (AC or DC mode is available)
- Support LC bridge function in series/parallel (Taiwan patent no.: 456205, 201430354)
- Calculable D/Q/ESR/ $\theta$  for LC bridge mode
- Four different test frequency are available: 100/120/1k/10k Hz for LC bridge measurement
- Test signal level:  $0.6V_{RMS}$  typ.
- 5 ranges used for LC bridge mode
- Test range: (Auto frequency configuration)
   L: 600.0 μH ~ 100.0 H (L<sub>S</sub>/L<sub>P</sub>)
   C: 6.000 nF ~2.00 mF (C<sub>S</sub>/C<sub>P</sub>)
- Low battery voltage detector
- Support buzzer sound driver control & frequency selectable
- Band-gap reference voltage output
- 3-wire serial bus for MCU I/O port
- MCU I/O power level selectable by external pins

#### Application

Handheld DMM with LC bridge meter

(US patent no.: 9176187)

(Taiwan patent no.: 458990)

# Description

The ES166 is the analog frond end chip for DMM with LC suitable bridge measurement function. ES166 provides basic voltage & current (AC/DC) measurement, resistance measurement, diode check, fast continuity measurement. frequency measurement, and duty cycle measurement. By using ES166 to implement the LC bridge function, the complicated PCB design is not necessary. The ES166 is built-in resistor switches network to provide different ranges control. It also provides a high performance integrated circuit to generate sinusoidal signal with different frequency to measure the complex impedance of DUT device. The ES166 includes a flexible serial interface to external MCU. The MCU could get the real part and imaginary part of complex impedance from ES166 directly and calculates the  $D/O/ESR/\theta$  parameter easily with L or C values. The MCU could get the DMM data from ES166 by each DMM measurement function mode also.



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# **Absolute Maximum Ratings**

Characteristic	Rating
Supply Voltage (V- to AGND)	-4V
Analog Input Voltage	V0.6 to V+ +0.6
V+	$V+ \ge (AGND/DGND+0.5V)$
AGND/DGND	$AGND/DGND \ge (V - 0.5V)$
Digital Input (IO_CTRL=V-)	V0.6 to uPVCC+0.6
Power Dissipation. Flat Package	500mW
Operating Temperature	-20°C to 70°C
Storage Temperature	-55°C to 125°C

# **Electrical Characteristics**

					111-2.	<u> </u>
Power supply	V-	Test condition	-2.2	-3.0	-3.4	V
	I <sub>DD</sub>	DCV mode	_	1.4	_	mA
Operating supply current	I <sub>DD</sub>	LC mode	_	3.6	_	mA
	I <sub>SS</sub>	In sleep mode	_	1	3	μΑ
Voltage roll-over error		$10M\Omega$ input resistor		—	±0.1	% F.S <sup>1</sup>
ADC nonlinearity <sup>2</sup>		Best case straight line	_	—	±0.1	%F.S <sup>1</sup>
ADC full scale range		$VR_VA = -400mV$	—	600	_	mV
Input Leakage for VR1 input			-10	1	10	pА
Zero input reading		$10M\Omega$ input resistor	-000	000	+000	Count
Band-gap reference voltage	$V_{\rm RH}$	100KΩ resistor between VRH and AGND	-1.30	-1.22	-1.14	v
Source voltage for diode mode			—	V+	_	V
Open circuit voltage for $600\Omega$ range measurement			_	V-	_	v
Open circuit voltage for other $\Omega$ measurement				-0.9		v
Internal pull-high to 0V current		Between V- pin and CS	_	1.2	_	μA
AC frequency response at 6.000V		±1%		40-400	_	
range		±5%	_	400-2000	_	HZ
STBEEP comparator in Cont./Diode mode		OVX to SGND	_	<u>+</u> 7	_	mV
Frequency input sensitivity (FREQ)	Fin	Square wave with Duty cycle 40-60%	500	—	_	mVp
Frequency input sensitivity (FREQ)	Fin	Sine wave	400	_	_	mVrms
Low battery flag indication		Connect LBAT to AGND	-2.2	-2.3	-2.4	v
Best basic accuracy for LC mode	Ae	100-10k $\Omega$ range	_		±0.5	%

 $TA=23 + 5^{\circ}C$ 



# ES166 LCR/DMM analog front

Test signal amplitude (LC mode)		$R_{DUT}=100k\Omega$ $VR\_LC = -600mV$	_	0.6	_	V <sub>RMS</sub>
Reference voltage temperature coefficient	TC <sub>RF</sub>	100KΩ resister Between VRH -20°C <ta<70°c< td=""><td> </td><td>75</td><td>150</td><td>ppm/°C</td></ta<70°c<>		75	150	ppm/°C

Note:

1. Full Scale :6000 counts (Max. 6784<u>+</u>2 counts)

2. For best integral linearity of ADC, the metalized polypropylene film capacitor for CINT is necessary.

#### **AC** electrical characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit
SCLK clock frequency	f <sub>SCLK</sub>	-	-	100	kHz
SCLK clock time "L"	t <sub>LOW</sub>	4.7	-	-	
SLCK clock time "H"	t <sub>HIGH</sub>	4.0	-	-	us
SDATA output delay time	t <sub>AA</sub>	0.1	-	3.5	
SDATA output hold time	t <sub>DH</sub>	100	-	-	ns
Start condition setup time	t <sub>SU.STA</sub>	4.7	-	-	110
Start condition hold time	t <sub>HD.STA</sub>	4.0	-	-	us
Data input setup time	t <sub>SU.DAT</sub>	200	-	-	
Data input hold time	t <sub>HD.DAT</sub>	0	-	-	118
Stop condition setup time	t <sub>SU.STO</sub>	4.7	-	-	
SCLK/SDATA rising time	t <sub>R</sub>	-	-	1.0	
SCLK/SDATA falling time	t <sub>F</sub>	-	-	0.3	us
Bus release time	t <sub>BUF</sub>	4.7	-	-	

# MCU I/O timing diagram





# 1. Functional description

#### 1.1 Overview

The ES166 is an analog front end IC built-in multiple measurement modes for digital multi-meter application. It is built-in basic multi-meter measurement modes which includes AC/DC voltage, AC/DC current, resistance, diode check, continuity, frequency modes, and so on. It is also built-in the LC bridge mode which could measure complex impedance (Inductance/Capacitance) directly with secondary parameters including dissipation factor (D), quality factor (Q), phase angle ( $\theta$ ), equivalent series or parallel resistance (R<sub>S</sub> or R<sub>P</sub>). The ES166 also provides a flexible serial interface for external microprocessor operation. The external microprocessor could implement a fully auto range DMM product by proper firmware design with ES166.

#### 1.2 Microprocessor serial I/O

ES166 configures a 3-wire serial I/O interface to external micro-controller (MCU). The SDATA pin is bi-directional and SCLK & DATA\_NEW are unilateral. The SDATA pin is configured by open-drain circuit design. The DATA\_NEW is used to check the data buffer of ADC ready or not. When the ADC conversion cycle is finished, the DATA\_NEW pin will be pulled high until MCU send a valid read command to ES166. After the first ID byte of read command is confirmed, the DATA\_NEW will be driven to low until the next ADC conversion finished again.

The data communication protocol is shown below. The write protocol is configured by an ID byte with 5 command bytes following. The read protocol is configured by an ID byte with 20 data bytes as followed.

#### Write command:

ID byte, Write control byte1, Write control byte2, Write control byte3, Write control byte4 and Write control bytes5.





# Read command:

ID byte, Read data byte1, Read data byte2 ~ Read data byte19, Read data byte20



The ID byte of ES166 is header of "110010" followed by a buzzer on/off control bit and R/W bit. The start/stop bit definition is shown on the diagram below.





#### 1.3 Read/Write command description

The write command includes one ID byte with five command bytes. If the valid write ID code is received by ES166 at any time, the write command operation will be enabled.

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID	1	1	0	0	1	0	BUZ	R/W=0
W1	F3	F2	F1	FO	AC	Q2	Q1	Q0
W2	FQ2	FQ1	FQ0	BO	<b>B</b> 1	B2	0	IOP1
W3	SHBP	0	0	0	0	0	0	0
W4	AVG	0	PG0	PG1	FG0	FG1	RR0	RR1
W5	0	0	0	0	0	0	0	0

The next table shows the content of write command.

Note: The W5 control byte is a test mode command. Please send zero word at normal operation.

Auxiliary low-resistance detection control bit for Continuity and Diode modes: SHBP

Measurement function control bit: F3/F2/F1/F0

Range control bit for V/A/R modes: Q2/Q1/Q0

Range control bit for Frequency mode: FQ2/FQ1/FQ0

Buzzer frequency selection: **B2/B1/B0** 

Buzzer driver ON/OFF control bit: BUZ

AC mode control enable bit: AC

OP configuration control bit: **IOP1** 

LC bridge data output smoothing: AVG (Recommend AVG=1)

Range control bit for L/C mode: RR1/RR0/PG1/PG0

Test signal frequency control bit for LC bridge mode: FG1/FG0



After write operation is enable, the internal ADC timing will be reset. The first allowed ADC data will be ready when the DATA\_NEW is high. The read command includes one ID byte with 20 data bytes. When DATA\_NEW is ready, MCU could send the read data command to get the result of ADC conversion  $(D0/D1/D2^1 \& A/B/C^2)$  or status flag from ES166.

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID	1	1	0	0	1	0	BUZ	R/W=1
R1	ALARM	DRDY	SIGN	LBAT	STA0	STA1	F_FIN	LDUTY
R2	HF	LF	OLD	D0:12	D0:11	D0:10	D0:09	D0:08
R3	D0:07	D0:06	D0:05	D0:04	D0:03	D0:02	D0:01	D0:00
R4	D1:19	D1:18	D1:17	D1:16	D1:15	D1:14	D1:13	D1:12
R5	D1:11	D1:10	D1:09	D1:08	D1:07	D1:06	D1:05	D1:04
R6	D1:03	D1:02	D1:01	D1:00	D2:19	D2:18	D2:17	D2:16
R7	D2:15	D2:14	D2:13	D2:12	D2:11	D2:10	D2:09	D2:08
R8	D2:07	D2:06	D2:05	D2:04	D2:03	D2:02	D2:01	D2:00
R9	A <sub>31</sub>	A <sub>30</sub>	A <sub>29</sub>	A <sub>28</sub>	A <sub>27</sub>	A <sub>26</sub>	A <sub>25</sub>	A <sub>24</sub>
R10	A <sub>23</sub>	A <sub>22</sub>	A <sub>21</sub>	A <sub>20</sub>	A <sub>19</sub>	A <sub>18</sub>	A <sub>17</sub>	A <sub>16</sub>
R11	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>	A <sub>11</sub>	$A_{10}$	A <sub>09</sub>	$A_{08}$
R12	A <sub>07</sub>	$A_{06}$	A <sub>05</sub>	A <sub>04</sub>	A <sub>03</sub>	$A_{02}$	A <sub>01</sub>	$A_{00}$
R13	<b>B</b> <sub>31</sub>	<b>B</b> <sub>30</sub>	B <sub>29</sub>	<b>B</b> <sub>28</sub>	<b>B</b> <sub>27</sub>	B <sub>26</sub>	<b>B</b> <sub>25</sub>	<b>B</b> <sub>24</sub>
R14	<b>B</b> <sub>23</sub>	<b>B</b> <sub>22</sub>	<b>B</b> <sub>21</sub>	B <sub>20</sub>	<b>B</b> <sub>19</sub>	<b>B</b> <sub>18</sub>	<b>B</b> <sub>17</sub>	<b>B</b> <sub>16</sub>
R15	<b>B</b> <sub>15</sub>	<b>B</b> <sub>14</sub>	<b>B</b> <sub>13</sub>	<b>B</b> <sub>12</sub>	<b>B</b> <sub>11</sub>	<b>B</b> <sub>10</sub>	B <sub>09</sub>	<b>B</b> <sub>08</sub>
R16	B <sub>07</sub>	<b>B</b> <sub>06</sub>	<b>B</b> <sub>05</sub>	<b>B</b> <sub>04</sub>	<b>B</b> <sub>03</sub>	B <sub>02</sub>	<b>B</b> <sub>01</sub>	<b>B</b> <sub>00</sub>
R17	C <sub>31</sub>	C <sub>30</sub>	C <sub>29</sub>	C <sub>28</sub>	C <sub>27</sub>	C <sub>26</sub>	C <sub>25</sub>	C <sub>24</sub>
R18	C <sub>23</sub>	C <sub>22</sub>	C <sub>21</sub>	C <sub>20</sub>	C <sub>19</sub>	C <sub>18</sub>	C <sub>17</sub>	C <sub>16</sub>
R19	C <sub>15</sub>	C <sub>14</sub>	C <sub>13</sub>	C <sub>12</sub>	C <sub>11</sub>	C <sub>10</sub>	C <sub>09</sub>	C <sub>08</sub>
R20	C <sub>07</sub>	C <sub>06</sub>	C <sub>05</sub>	C <sub>04</sub>	C <sub>03</sub>	C <sub>02</sub>	C <sub>01</sub>	C <sub>00</sub>

The next table shows the content of read command.

DATA\_NEW for frequency or capacitance mode will be active when D0 or D3 data ready.

<sup>1</sup>Note: **D0/D1/D2** all are binary code format. **SIGN** is signed status bit indication for **D0** only.

<sup>2</sup>Note: The *A* ( $A_{31}$ - $A_{00}$ ), *B* ( $B_{31}$ - $B_{00}$ ), *C* ( $C_{31}$ - $C_{00}$ ) are 32-bit 2's complement signed integer which could be accessed from ES166 sequentially during read mode. The L/C impedance could be derived from the three numbers and calculated by external MCU easily.



F3	F2	F1	F0	Measurement mode	Read data bytes
0	0	0	0	V mode/ VHz mode	D0(12-00), D1(19-00), D2(19-00)
0	0	0	1	A mode / AHz mode	D0(12-00), D1(19-00), D2(19-00)
0	0	1	0	Resistance mode	D0(12-00)
0	0	1	1	Continuity mode	D0(12-00)
0	1	0	0	Diode check mode	D0(12-00)
0	1	0	1	Frequency/Duty cycle	D1(19-00), D2(19-00)
0	1	1	0	LC impedance mode	A(31-00),B(31-00),C(31-00)
0	1	1	1	ADP1/ Hz mode	D0(12-00), D1(19-00), D2(19-00)
1	0	0	0	ADP2 mode	D0(12-00)

The ADC data output for measurement mode: F3/F2/F1/F0

#### Buzzer frequency selection: B2/B1/B0

B2	B1	B0	Buzzer frequency
0	0	0	1.00kHz
0	0	1	1.33kHz
0	1	0	2.00kHz
0	1	1	2.22kHz
1	0	0	2.67kHz
1	0	1	3.08kHz
1	1	0	3.33kHz
1	1	1	4.00kHz

Set B2-B0 properly to get the target frequency. Set **BUZ** control bit or drive *BUZIN* (pin 15) to enable/disable the *BUZOUT* (pin12) driver output. If MCU control BUZ only, it is available to set ID byte with ending of stop bit.





Status flags for me	asurement	mode: <ul> <li>mode:</li> </ul>	= function a	available	
Measurement mode	ALARM	SIGN	LBAT	STA0	STA1
V mode					
V+Hz mode			•		•
A mode			•		
A+Hz mode					
Resistance mode			•		
Continuity mode			•		
Diode check mode			•		
Freq. + duty mode			•		•
LC bridge Mode			•		
ADP1/ADP2 mode			•		
ADP1+Hz mode			•		•
Measurement mode	F_FIN	LDUTY	HF	LF	OLD
V mode					
V+Hz mode					
A mode					
A+Hz mode					
Resistance mode					
Continuity mode					
Diode check mode		-		-	
Freq. + duty mode					
LC bridge Mode					
ADP1/ADP2 mode					
ADP1+Hz mode					

**Description of status flags:** 

SIGN: Sign bit of D0 output (Data = -1 \* D0 if SIGN=1)

LBAT: Low battery voltage indication

ALARM: High crest factor signal detection in ACV mode or Short detected in Continuity/Diode mode

HF: Higher frequency indication for Hz mode

LF: Lower frequency indication for Hz mode

LDUTY: Low duty indication for duty cycle mode

STA0/STA1: divider indication for Hz mode

F\_FIN: Measurement cycle finished for Hz mode

OLD: DUT Overflow indication for LC bridge mode



#### 1.4 Power & I/O level selection

The ES166 provide a flexible I/O level setting for different MCU system configuration. The uPVCC (pin19) should be connected to the same potential of external Vcc of MCU. The uPVCC is allowed to be set between DGND ~ V+. The *IOCTRL* (pin14) selects the Vss level of MCU. If *IOCTRL* is set to DGND, the Vss level of MCU is the same as DGND. If *IOCTRL* is set to V-, the Vss level of MCU is the same as V-.







#### 1.5 Basic impedance theory

The general DMM could measure DC resistance only, but the LCR meter could measure AC impedance. The impedance consists of resistance (real part) and reactance (imaginary part). For example, Zs represents the impedance in series mode. Zs can be defined a combination of resistance Rs and reactance Xs. It also could be defined as a |Z| of magnitude with a phase angle  $\theta$ .



There are two types for reactance. The one is the inductive reactance  $X_L$  and the other is the capacitive reactance  $X_C$ . They could be defined as: (*f* = test signal frequency)  $X_L = 2 \pi f L$  (L = Inductance)

$$X_{\rm C} = \frac{1}{2 \pi f C}$$
 (C = Capacitance)



#### **1.6 LC impedance measurement mode**

The impedance could be measured in series or parallel mode. The impedance *Z* in parallel mode could be represented as reciprocal of admittance *Y*. The admittance could be defined as Y = G + jB. The G is the conductance and the B is the susceptance.

Impedance in serial mode



Rs: Resistance in series mode Xs: Reactance in series mode Cs: Capacitance in series mode Ls: Inductance in series mode



Y = 1/Z = 1/Rp + 1/jXp = G + jBRp: Resistance in parallel mode Xp: Reactance in parallel mode Cp: Capacitance in parallel mode Lp: Inductance in parallel mode

There are two factors to provide the ratio of real part and imaginary part. Usually the quality factor Q is used for inductance measurement and the dissipation factor D is used for capacitance measurement. D factor is defined as a reciprocal of Q factor.

 $Q = 1 / D = \tan\theta$   $Q = Xs / Rs = 2 \pi f Ls / Rs = 1 / 2 \pi f Cs Rs$  $Q = B / G = Rp / |Xp| = Rp / 2 \pi f Lp = 2 \pi f Cp Rp$ 

Actually, Rs and Rp are existed in the equivalent circuit of capacitor or inductor. If the capacitor is small, Rp is more important than Rs. If capacitor is large, the Rs is also more important. Therefore, use parallel mode to measure lower value capacitor and use series mode to measure higher value capacitor. For inductor, the impedance relationship is different from capacitor. If the inductor is small, Rp is almost no effect. If inductor is large, the Rs is also no effect. Therefore, use series mode to measure lower value inductor and use parallel mode to measure higher value inductor.



# 2. Operating Modes

#### 2.1 Voltage Measurement

MCU send write command to select the voltage measurement function. The Hz mode measurement is available to be enabled with the ACV function (set AC bit to 1) simultaneously. The measured signal is applied to VRI terminal (pin75) through 10M $\Omega$ .

See the next table of function command:

F3	F2	F1	FO	AC	Measurement mode	Read data bytes
0	0	0	0	0	DCV mode	D0(12-00)
0	0	0	0	1	ACV+Hz mode	D0(12-00), D1(19-00), D2(19-00)

Note1: D0/D1/D2 all are binary format. SIGN are the sign bit of D0.

Range control for voltage mode (ACV/DCV)

Q2	Q1	Q0	Full Scale Range	<b>Divider Ratio</b>	<b>Resister Connection</b>
0	0	0	6.000V	1/10	VR2 (1.111MΩ)
0	0	1	60.00V	1/100	VR3 (101kΩ)
0	1	0	600.0V	1/1000	VR4 (10.01kΩ)
0	1	1	1000V	1/10000	VR5 (1kΩ)
1	0	0	600.0mV	1	VR1 (10MΩ)

Note: For consideration of frequency bandwidth and noise immunity, use ADP1 mode implement mV range is better.

Frequency range control for ACV+Hz mode

FQ2	FQ1	FQ0	Full Scale Range
0	0	0	N/A
0	0	1	600.0Hz
0	1	0	6.000kHz
0	1	1	60.00kHz

Note: See frequency mode (section 2.6) also. If AC value is less than 1% full scale, the Hz count should be set to zero by MCU directly.

ALARM bit at voltage mode is used for high crest factor (HCF) signal detection. If MCU check the ALARM status flag active when data and range are stable, it should consider the making the existing range up to avoid the signal clamping saturation caused by HCF signal. There is higher peak voltage with lower RMS value for HCF signal. So if the range is up according to the ALARM bit, MCU should set the lower under-limit counts temporarily to avoid the ranging unstable for this case.



#### 2.2 Current measurement

MCU send write command to select the current measurement function. The Hz mode measurement is available to be enabled with the ACA function (set **AC** bit to 1) simultaneously. The measured signal is applied to *IVS* terminal (pin4).

See the next table of function command:

F3	F2	F1	FO	AC	Measurement mode	Read data bytes
0	0	0	1	0	DCA mode	D0(12-00)
0	0	0	1	1	ACA+Hz mode	D0(12-00),D1(19-00),D2(19-00)

Note1: D0/D1/D2 all are binary format. SIGN are the sign bit of D0.

Range control for current mode (ACA/DCA)

Q2	Q1	Q0	IOP1 <sup>2</sup>	Full Scale Range	Input terminal
0	0	0	1	$30.00 \text{mV} \rightarrow 6000 \text{counts}$	$IVS^1$
0	0	0	0	$300.0 \text{mV} \rightarrow 6000 \text{counts}$	$IVS^1$

<sup>1</sup>Note: The maximum burden voltage for current mode will be 300mV.

<sup>2</sup>Note: When IOP1=1, the DC zero offset and AC gain should be calibrated by MCU in production.

FQ2	FQ1	FQ0	Full Scale Range
0	0	0	N/A
0	0	1	600.0Hz
0	1	0	6.000kHz
0	1	1	60.00kHz

Note: See frequency mode (section 2.6) also. If AC value is less than 1% full scale, the Hz count should be set to zero by MCU directly.



#### 2.3 Resistance Measurement

MCU send write command to select the dc resistance measurement function.

F3	F2	F1	FO	Measurement mode	Read data bytes
0	0	1	0	Resistance mode	D0(12-00)

Note1: D0 is binary format. SIGN bit could be ignored.

Range control for resistance mode

Q2	Q1	Q0	Full Scale Range	<b>Relative Resistor</b>	Equivalent value
0	0	0	N/A	N/A	N/A
0	0	1	600.0Ω	OR1	100Ω
0	1	0	6.000KΩ	VR5	1ΚΩ
0	1	1	60.00KΩ	VR4    VR1	10KΩ
1	0	0	600.0KΩ	VR3    VR1	100KΩ
1	0	1	6.000MΩ	VR2    VR1	1ΜΩ
1	1	0	60.00MΩ	VR1	10ΜΩ

#### 2.4 Continuity measurement

MCU send write command to select the continuity measurement function.

F3	F2	F1	FO	Measurement mode	Read data bytes
0	0	1	1	Continuity mode	D0(12-00)

Note1: D0 is binary format. SIGN bit could be ignored.

Continuity mode shares the same configuration with  $600.0\Omega$  resistance measurement circuit and support the low-resistance detection. If the *STBEEP* output (pin11) is low, it means the low-resistance status is detected (It means the *OVX* terminal voltage less than -7mV). So MCU could monitor the *STBEEP* output and ADC (D0) data output make the high speed detection for continuity check. Set **SHBP**=1 to enable the built-in buzzer driving automatically when *STBEEP* is active. In this case, the ALARM bit is active also.



#### 2.5 Diode Measurement

MPU send write command to select the diode measurement function.

F3	F2	F1	FO	Measurement mode	Read data bytes
0	1	0	0	Diode check mode	D0(12-00)

Note1: D0 is binary format. SIGN is the sign bit of D0.

Diode measurement mode shares the same configuration with 6.000V voltage measurement circuit and support the low-resistance detection. If the *STBEEP* output (pin11) is low, it means the low-resistance status is detected (It means the *OVX* terminal voltage less than 7mV). So MCU could monitor the *STBEEP* output and ADC (D0) data output make the high speed detection for short circuit detection. Set **SHBP**=1 to enable the built-in buzzer driving automatically when *STBEEP* is active. In this case, the ALARM bit is active also.

#### 2.6 Frequency/duty cycle mode measurement

The default typical input impedance of frequency with duty cycle mode is  $100k\Omega$ . The MCU send write command to select the frequency/duty cycle measurement function.

F3	F2	F1	FO	Measurement mode	Read data bytes
0	1	0	1	Hz + Duty mode	D0(12-00), D1(19-00), D2(19-00)

Note1: D0/D2/D3 all are binary format. ASIGN bit is ignored.

150	contro	1 101 11	equene	y mode
	FQ2	FQ1	FQ0	Full Scale
	0	0	0	N/A
	0	0	1	600.0Hz
	0	1	0	6.000KHz
	0	1	1	60.00KHz
	1	0	0	600.0KHz
	1	0	1	6.000MHz

0

Range control for frequency mode

20.00MHz



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Flag	STA 0-1	STA	<b>10=0</b>		
Range	51AU=1	STA1=1	STA1=0		
600.0Hz	FREQ=1000000/D2	FREQ=8000000/D2	FREQ=64000000/D2		
6.000KHz	FREQ=2000000/D2	FREQ=8000000/D2	FREQ=51200000/D2		
60.00KHz					
600.0KHz	FREQ = D0 (FREQ= D2 if V/A +Hz mode)				
6.000MHz					
20.00MHz					

Status Flag	LDUTY=1	LDUTY=0
Duty cycle (<60kHz)	1000-D1*1000/D2	D1*1000/D2

The status flag F\_FIN indicate whether the frequency input signal is available (larger than  $F_{MIN}$ =1.0Hz) or not. If the computed result less than  $F_{MIN}$ , the frequency/duty cycle readings should be set to zero.

The status flags HF & LF are used for fast judgment of proper range. If frequency input is larger than 12 kHz, HF will be active. If frequency input is floating or frequency is detected too low, LF will be active.

A 4		a a maid a ma	Alar far		b			of fue or		
AIIIA	гяпое	considera	11061101	VIPI	nv usi	no siain	S HIMOS	or rea	nencv	mone
1 uu	iange	complacia	uon ioi		by ubl	ing Diata	JIIII	or meq	ucity	moue

-		• •		•
Flag	F_FIN=0	F_FIN=1	F_FI	[N=1
Range	LF=0	LF=1*	HF=LF=0	HF=1**
600.0Hz		Hz/Duty=0		Set range to
6.000KHz	Data and		Change range	range
60.00KHz 600.0KHz 6.000MHz	Range is not necessary to be updated	Set range to 600.0Hz range	depends on data computed	Change range depends on
20.00MHz				uata computeu

\*Note: LF=1 @ 600Hz range implies the frequency is not available to be measured. The Hz/Duty readings should be set to zero simultaneously.

\*\*Note: When ACV+Hz/ACA+Hz/ADP+Hz mode is selected, the HF/LF status should be ignored. Change range depends on data calculation result. If AC value is less than 1% full scale, the Hz count should be set to zero by MCU directly.



Duty cycle mode range (Input sensitivity > 5Vpp @ duty cycle= 5.0% or 95.0%)

Freq. range	Duty range
60.00Hz 600.0Hz	5.0% - 95.0%
6.000KHz	10.0% - 90.0%
60.00KHz	20.0% - 80.0%

# 2.7 ADP mode

MCU send write command to select the ADP1 or ADP2 mode measurement function. The Hz mode measurement is available to be enabled with the ADP1 AC function (set AC bit to 1) simultaneously. The measured signal is applied to *ADP1in* terminal (pin5). The signal full scale is 600mV for DC mode and 600mVrms for AC mode.

See	the	next	table	of	function	command:

F3	F2	F1	FO	AC	Measurement mode	Read data bytes
0	1	1	1	0	ADP1 DC mode	D0(12-00)
0	1	1	1	1	ADP1 AC mode	D0(12-00), D2(19-00), D3(19-00)
1	0	0	0	0	ADP2 DC mode	D0(12-00)
1	0	0	0	1	ADP2 AC mode	D0(12-00)

Note1: D0/D1/D2 all are binary format. SIGN is the sign bit of D0.

-	U		
FQ2	FQ1	FQ0	Full Scale Range
0	0	0	N/A
0	0	1	600.0Hz
0	1	0	6.000kHz
0	1	1	60.00kHz

Frequency range control for ADP1/Hz mode

Note: See frequency mode (section 2.6) also. If AC value is less than 1% full scale, the Hz count should be set to zero by MCU directly.

MCU could control the IOP1 to reconfigure the full scale of ADC in ADP modes:

IOP1	ADC full scale in ADP mode
0	600.0mV
1	60.00mV



#### 2.8 Low battery detection

ES166 provides the low battery detection circuit for two cases. If 3V (1.5V\*2) battery is used, connect *LBAT* (pin53) terminal to *AGND* directly. The default typical low-battery threshold voltage is -2.3V (V- to AGND).

If more than 3V battery is used, the low battery status flag is active when the voltage of this pin is less than VRH voltage (Typ. -1.23V).

For examples:

9V battery configuration is used





#### 2.9 LC impedance mode

F3	F2	F1	FO	Measurement mode	Read data bytes
0	1	1	0	LC impedance mode	A(31-00), B(31-00), C(31-00)

Note: *A/B/C/D* is 32-bit signed integer. (2's complement binary number)

Measured in series mode Zs = Rs + jXs

In parallel mode:

$$C_P = C_S / (1+D^2)$$
  $L_P = L_S \ge (1+D^2)$   $R_P = R_S \ge (1+1/D^2)$ 

 $R_{Range}$  is defined by the external ratio resistor which could be selected by MCU write command.

Control bits				Torminal	Equivalent Range Resistor		
RR1	RR0	PG1	PG0	Terminai	$(\mathbf{R}_{\mathbf{RANGE}})$		
1	0	0	0	SW3	100kΩ		
0	1	0	0	SW2	10kΩ		
0	0	0	0	SW1	1kΩ		
0	0	0	1	SW1	100Ω		
0	0	1	0	SW1	10Ω		

f is the test frequency for LC impedance measurement which could be selected by MCU write command.

Cont	rol bits	$\mathbf{F}$
FG1	FG0	Frequency ( <i>J</i> )
0	0	100 Hz
0	1	120 Hz
1	0	1 kHz
1	1	10 kHz



#### 2.10 LC Scale Range

LC impedance mode					
Function mode	Frequency	Meas. Range	Min. resolution		
Inductance	100/120Hz	60.00mH~100.0H	0.01mH		
Inductance	1kHz	6000uH~60.00H	1uH		
Ls/Lp	10kHz	600.0uH~6.000H	0.1uH		
Capacitance	100/120Hz	60.00nF~ $2.00$ mF <sup>1</sup>	0.01nF		
	1kHz	6.000nF~600uF <sup>1</sup>	1pF		
Cs/Cp	$\frac{100}{100} Mean 000 Mean 0000 Mean 000 Mean 0$	600.0pF~60.0uF <sup>1</sup>	0.1pF		
	100/120Hz	60.00Ω~20.00ΜΩ	0.01Ω		
$R_{s}^{2}/R_{P}^{3}$	1kHz	60.00Ω~20.00MΩ	0.01Ω		
	10kHz	60.00Ω~20.00MΩ	0.01Ω		

Note:

<sup>1</sup>The max. range supports 0.01mF resolution & 1uF resolution & 0.1uF resolution, respectively. For better stable display, 0.1mF @ 100/120Hz is recommended. The 0.1pF resolution for Cp mode should be measured by test probe with good shielding.

 ${}^{2}R_{S}$  means equivalent series resistance for LC impedance measurement in series mode.

<sup>3</sup>R<sub>P</sub> means equivalent parallel resistance for LC impedance measurement in parallel mode.

For auto frequency	mode, the	best scale	range is shown	as the	following table	e:
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LC impedance mode							
Function mode	Auto frequency Meas. Range		Min. resolution				
Inductor	100Hz 15.90H~100.0H	0.01H					
Ls/Lp	1kHz	1590uH~15.90H	1uH				
	10kHz	0.0uH~1590uH	0.1uH				
Capacitance Cs/Cp	100Hz	15.90uF~2.0mF	0.01uF				
	1kHz	0.000nF~15.90uF	1pF				

In auto frequency mode, the measurement mode in series/parallel is also recommended to be automatic. Usually impedance  $Z_{DUT} \ge 10 k\Omega$  is in parallel and impedance  $Z_{DUT} < 10 k\Omega$  is in series defaulted.



# 2.11 Accuracy (Ae) vs. Impedance (Z<sub>DUT</sub>) @ Ta =18 ~ 28 $^{\circ}$ C

Freq. / Z	1 - 10Ω	$10 - 100\Omega$	$100-10k\Omega$	$10k - 100k\Omega$	$100k-20M\Omega$	Remark
100/120Hz	2.0%+3d	1.0%+2d	0.5%+1d	1.0%+2d	2.0%+3d	
1kHz	2.0%+3d	1.0%+2d	0.5%+1d	1.0%+2d	2.0%+3d	D < 0.1
10kHz	3.0%+3d	1.0%+2d	0.5%+1d	1.0%+2d	3.0%+3d	

Note:

• All accuracy is guaranteed by proper ratio resistor calibration and open/short calibration. All accuracy is guaranteed for 20cm distance from *DTH/DTL* pins of ES166.

If D > 0.1, the accuracy should be multiplied by  $\sqrt{1+D^2}$ 

 $Z_{\rm C} = 1/2 \pi f \, {\rm C} \quad \text{if } {\rm D} << 0.1 \text{ in capacitance mode}$  $Z_{\rm L} = 2 \pi f \, {\rm L} \qquad \text{if } {\rm D} << 0.1 \text{ in inductance mode}$ 

Ae = impedance (Z) accuracy

Definition:  $Q = \frac{1}{D}$ 

 $Rp = ESR (or Rs) \times (1 + \frac{1}{D^2})$ 

- 1. D value accuracy  $De = \pm Ae \times (1+D)$
- 2. ESR accuracy Re=  $\pm Z_M \times Ae(\Omega)$

ie.,  $Z_{\rm M}$  = impedance calculated by  $\frac{1}{2\pi fC}$  or  $2\pi f L$ 

3. Phase angle  $\theta$  accuracy  $\theta e = \pm (180/\pi) \times Ae (deg)$ 

# 4-terminals measurement with guard shielding

The DUT test leads are implemented by four terminals measurement. If four wires measurement is not possible, the accuracy of impedance less  $10\Omega$  should be increased properly. For achieve the accuracy shown above, it is necessary to do open/short calibration process before measurement. The test leads for DUT should be as short as possible. If longer extended cable or probe is used, the guard shielding is necessary. If guard shielding is not possible, the accuracy of impedance larger than  $100k\Omega$  should be increased properly.



# ES166 LCR/DMM analog front

# Package information (LQFP-80L / 10\*10)



#### VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.			
А		1.6			
A1	0.05	0.15			
A2	1.35	1.45			
c1	0.09	0.16			
D	12 BSC				
D1	10 BSC				
E	12 BSC				
E1	10 BSC				
е	0.4 BSC				
b	0.13	0.23			
L	0.45	0.75			
L1	1 REF				
	SYMBOLS A A1 A2 c1 D D1 E E1 E1 e b L L	SYMBOLS         MIN.           A            A1         0.05           A2         1.35           c1         0.09           D         12           D1         10           E         12           E1         10           e         0.4           b         0.13           L         0.45			

NOTES:

- 1.JEDEC OUTLINE:MS-026 BCE
- 2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
- 3.DIMENSION & DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM & DIMENSION BY MORE THAN 0.08mm.